

Compal Confidential

ULC AMD M/B LA-A996P DIS Schematics Document

AMD APU Beema/Kabini FT3 + ATI SUN LE + DDR3

Project Code : ZSO51

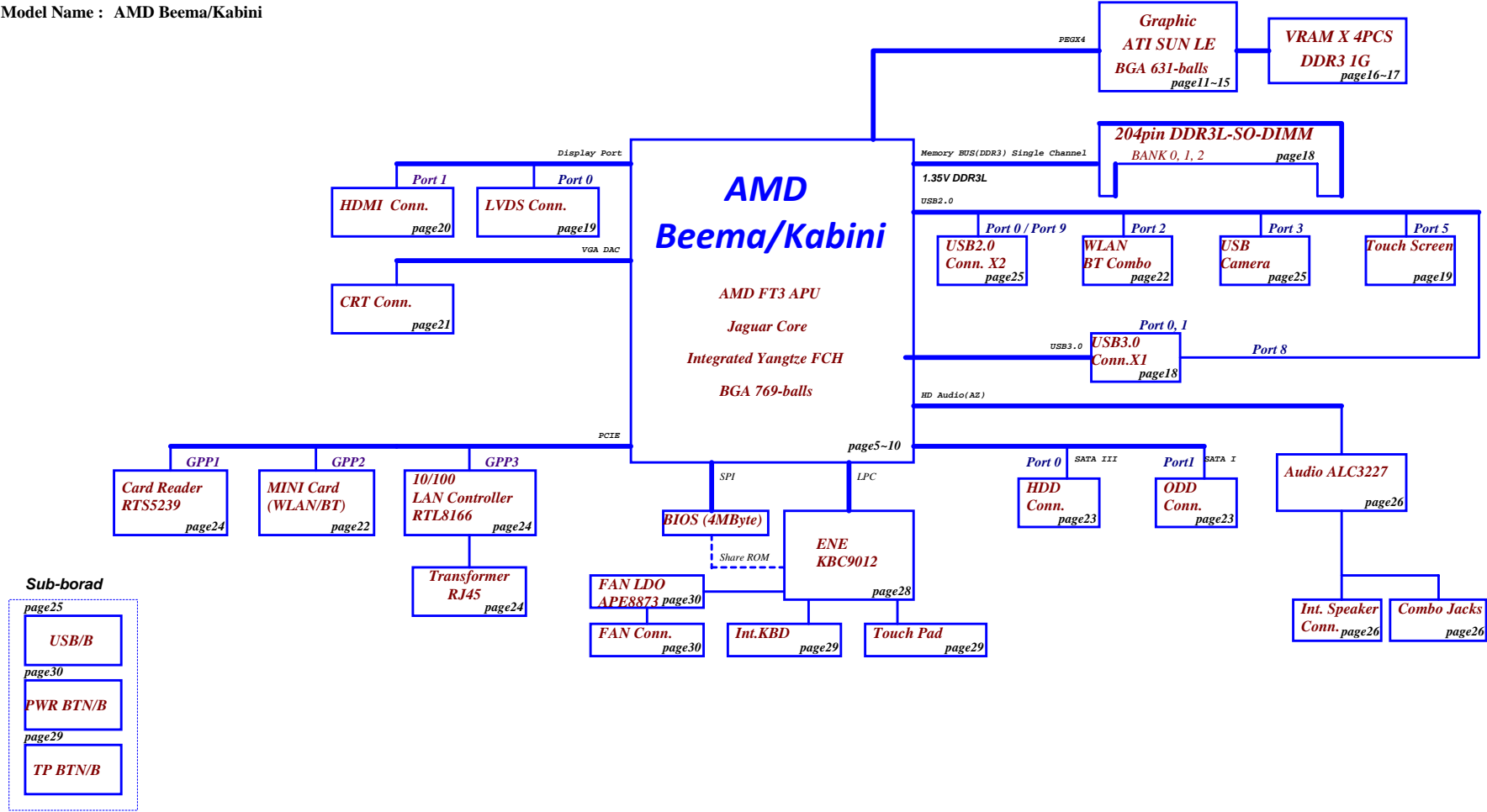
2014/02/08

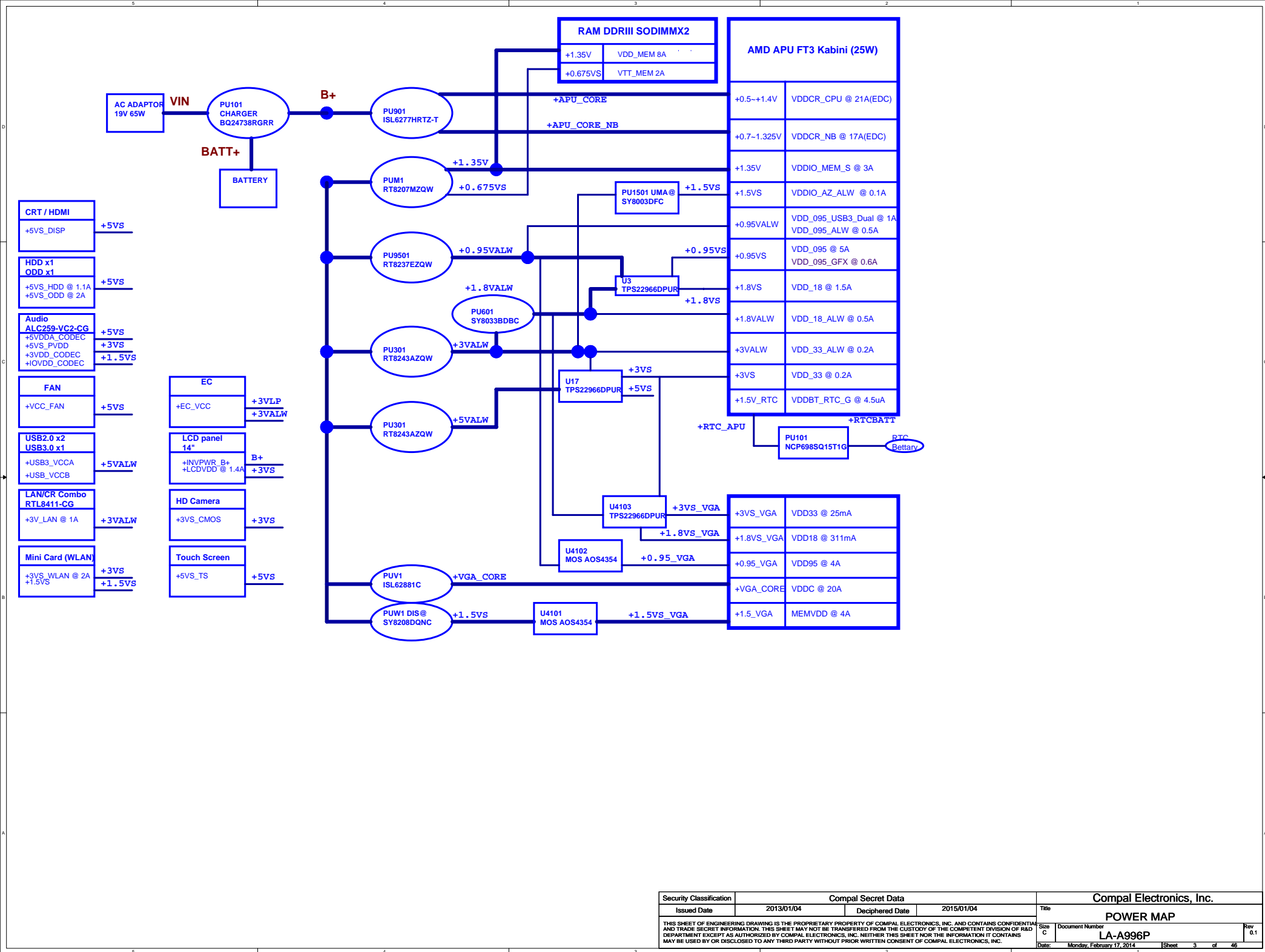
PV Rev. 4.0

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Model Name : AMD Beema/Kabini





Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power			

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF



A4-6300
Part Number = SA00007OP20
S IC A32 A4-6300 AM6300ITJ44JB



E2-6200
Part Number = SA00007OQ20
S IC A32 E2-6200 EM6200ITJ44JB 1.5G BGA



E1-6050
Part Number = SA00007IC50
S IC A32 E1-6050 ZM1332M2J2370 1.35G BGA



A8-6410 15W
Part Number = SA00007TQ20
AM6410ITJ44JB



A4-6210 R3 15W
Part Number = SA00007RA60
AM6210ITJ44JB



E2-6110 R2 15W
Part Number = SA00007RB60
EM6110ITJ44JB



E1-6010 R2 10
Part Number = SA00007RC60
EM6010IUJ23JB



A8-6410 15W
Part Number = SA00007TQ10
AM6410ITJ44JB



A4-6210 R1 15W
Part Number = SA00007RA40
AM6210ITJ44JB



E2-6110 R2 15W
Part Number = SA00007RB40
EM6110ITJ44JB



E1-6010 R2 10
Part Number = SA00007RC40
EM6010IUJ23JB



PCB
Part Number = DAZ14D00203
PCB LA-A996P REV4.0 M/B



E1-2100
Part Number = SA00006QX10
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A4-5000
Part Number = SA00006R410
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



E2-3800
Part Number = SA00007BX20
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A6-5200
Part Number = SA00006R350
S IC KABINI AM5200IAJ44HM 2G BGA769P APU



HDMI
Part Number = RO0000003HM
PCB 102 LA-A996P REV0 M/B 2



E1-2100
Part Number = SA00006QX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A4-5000
Part Number = SA00006R460
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



E2-3800
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SMBus List

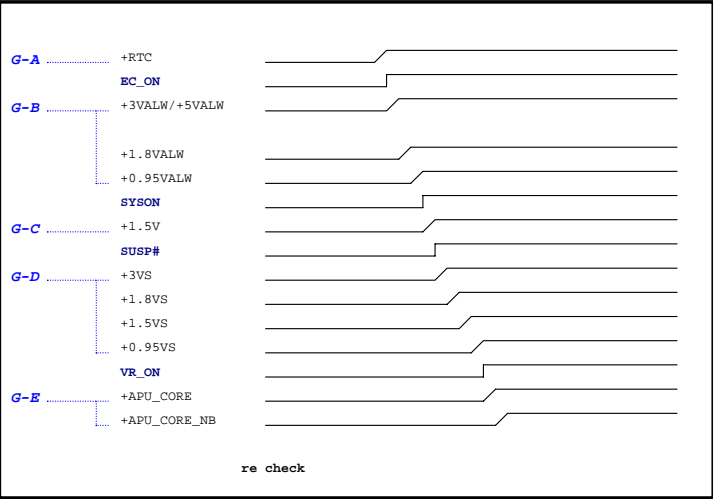
EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

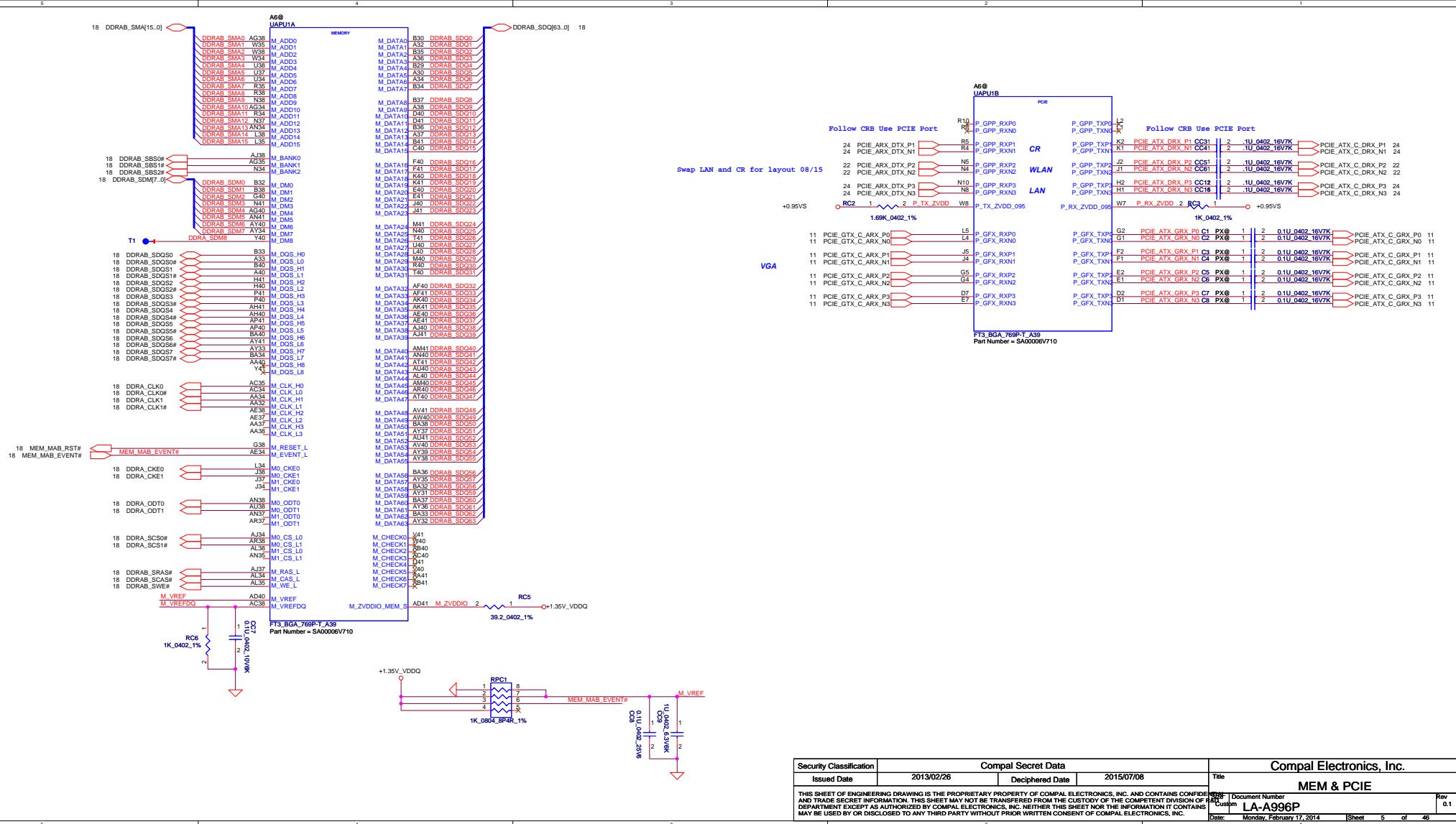
APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM2	1010 000Xb	A0H			
DDR DIMM1	1010 001Xb	A2H			
Mini Card (DNI)					

BOM Structure Table

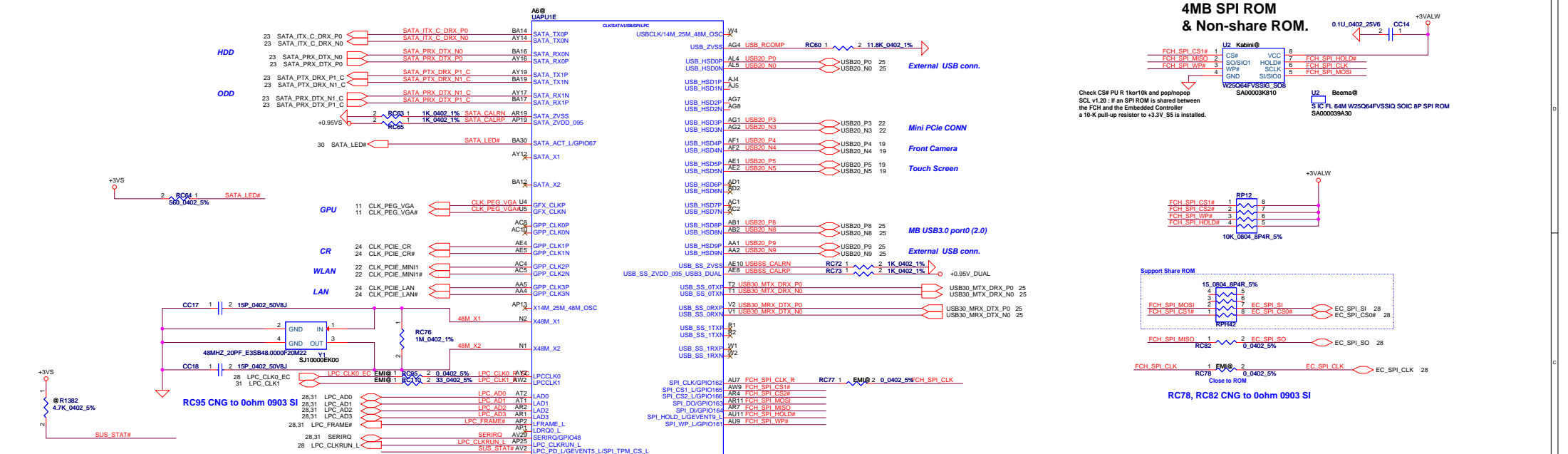
BOM Structure	BTO Item
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD Unpop component
PX@	GPU SUN LE Componet
8166@	10/100 LAN
8151@	Giga LAN
UMA@	UMA Componet
display@	display Componet
EDP@	EDP Componet
KLVDs@	Kabini LVDS Componet
BLVDs@	Beema LVDS Componet
Kabini@	Kabini Componet
Beema@	Beema Componet
LVDS@	LVDS Componet

APU POWER SEQUENCE



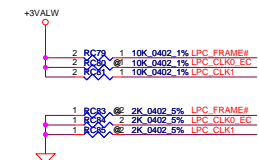


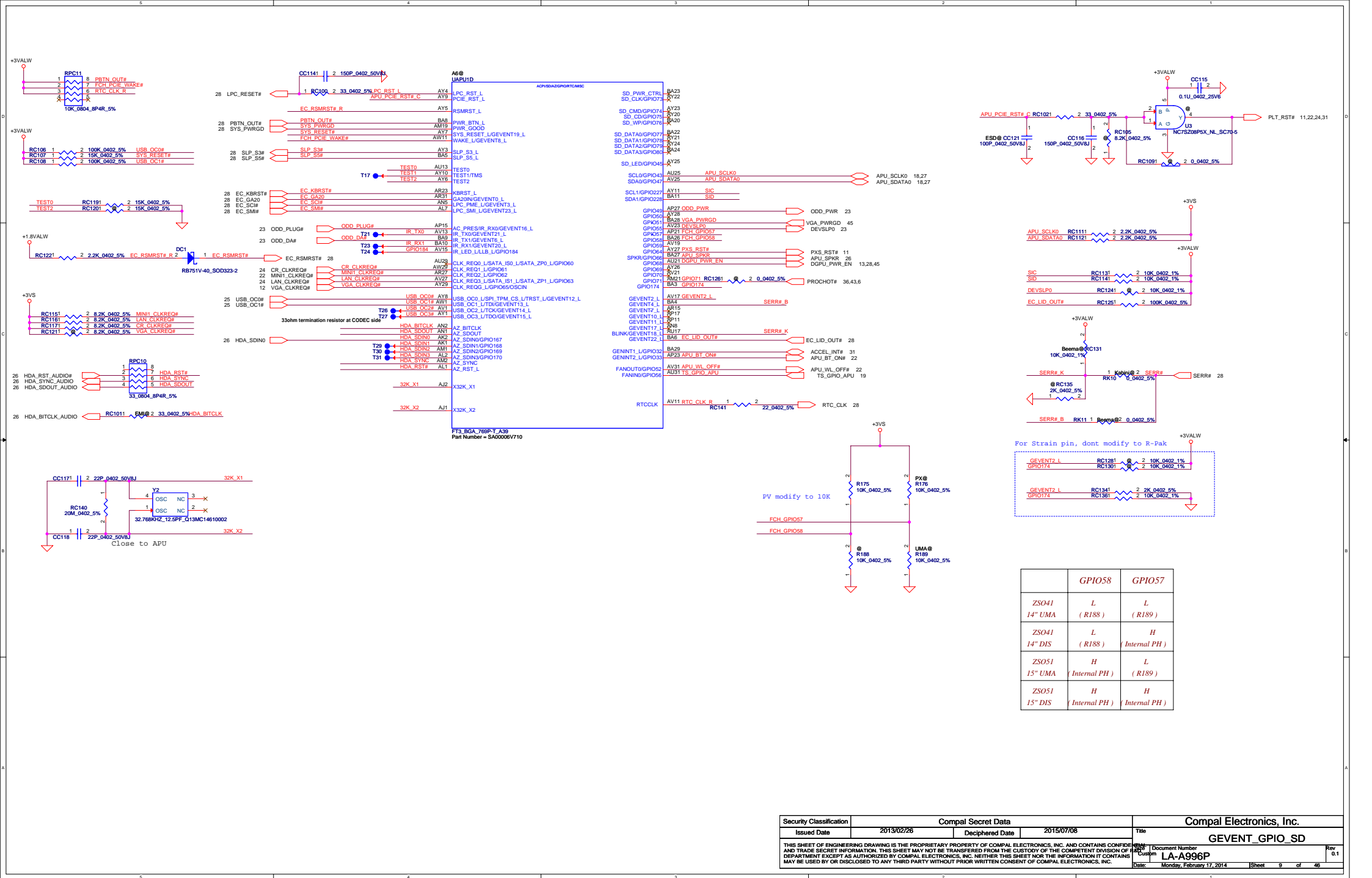
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			Document Number	Rev
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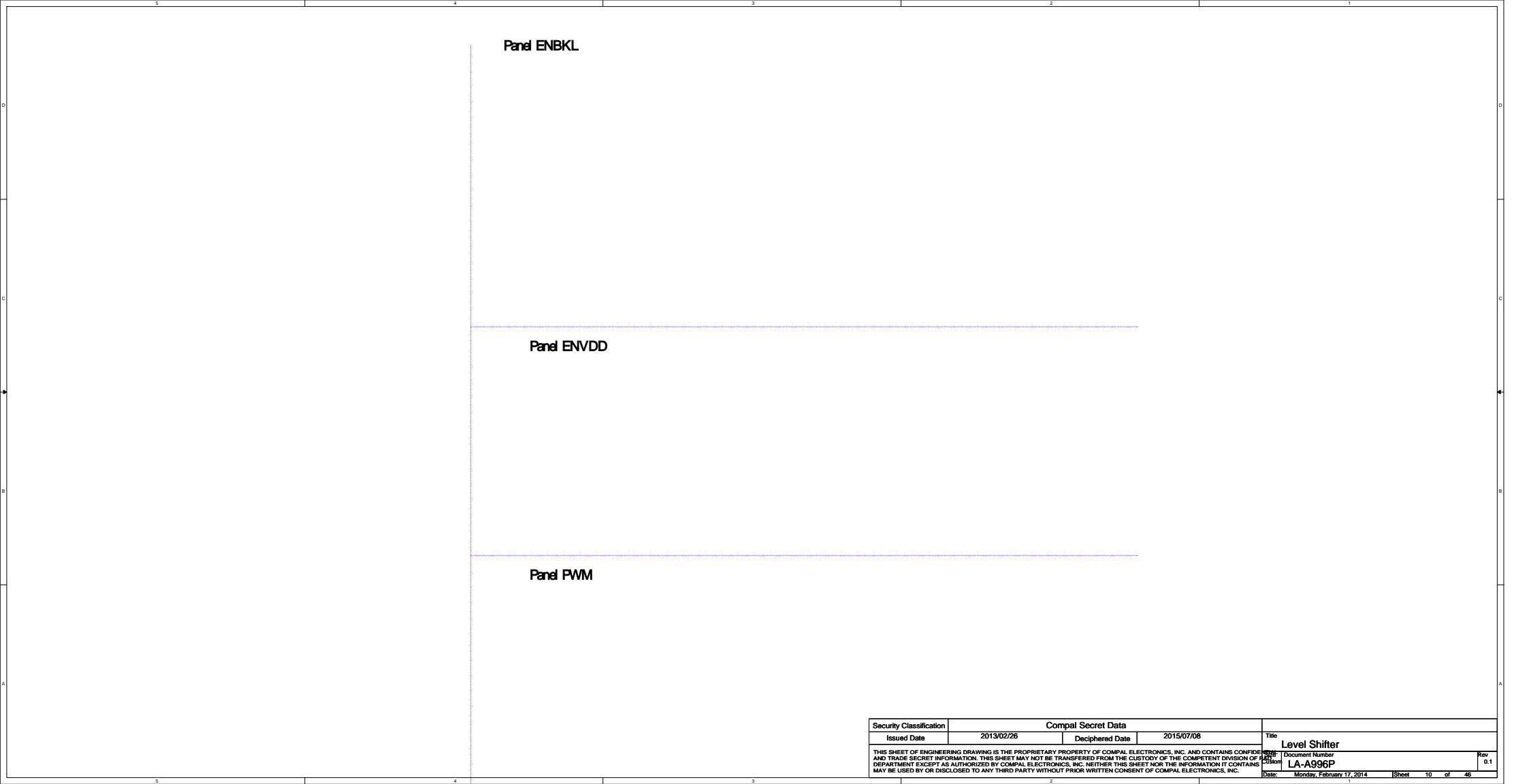


STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION





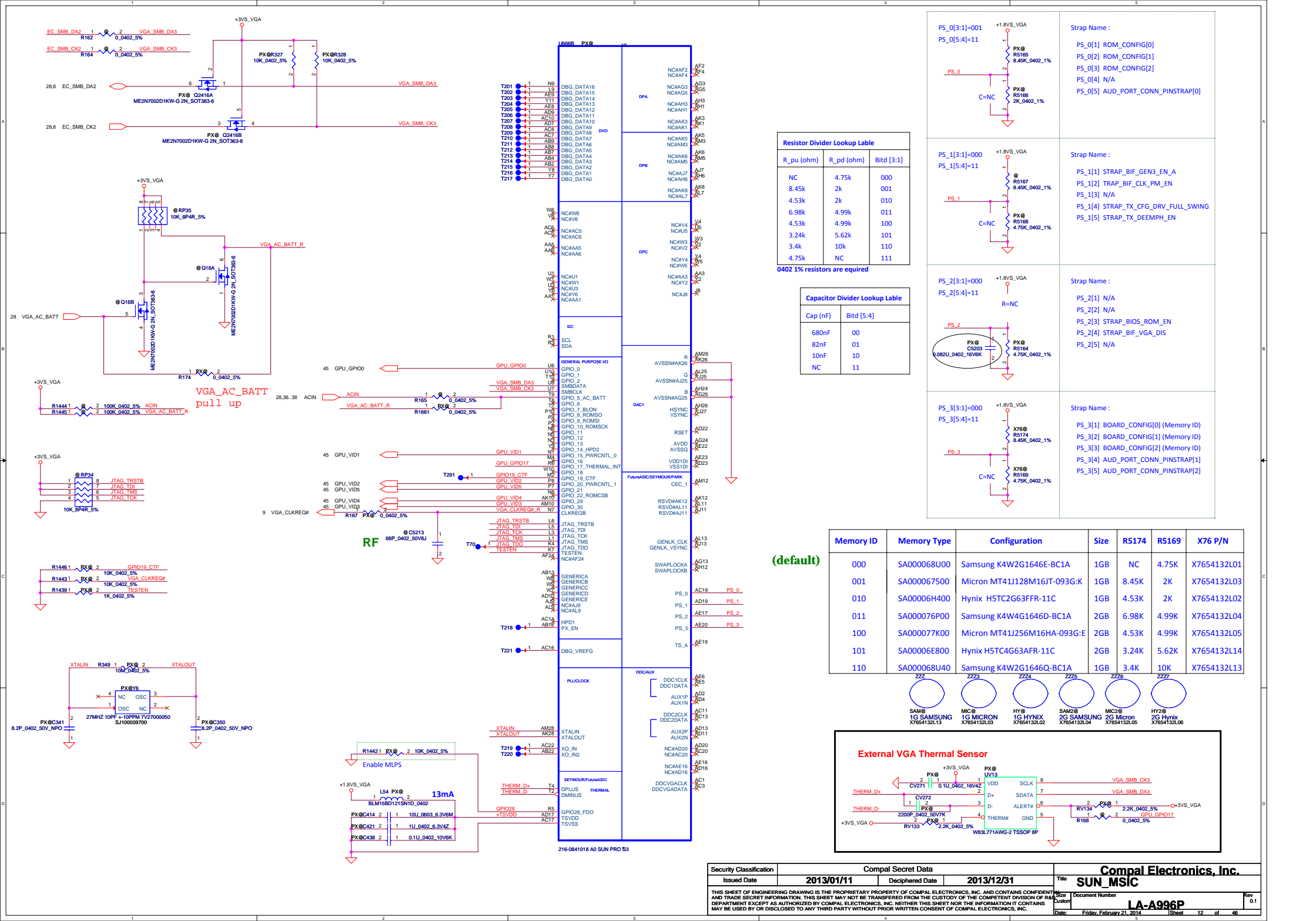


Panel ENBKL

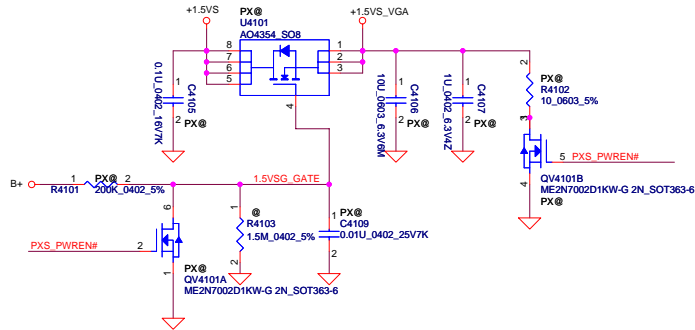
Panel ENVDD

Panel PWM

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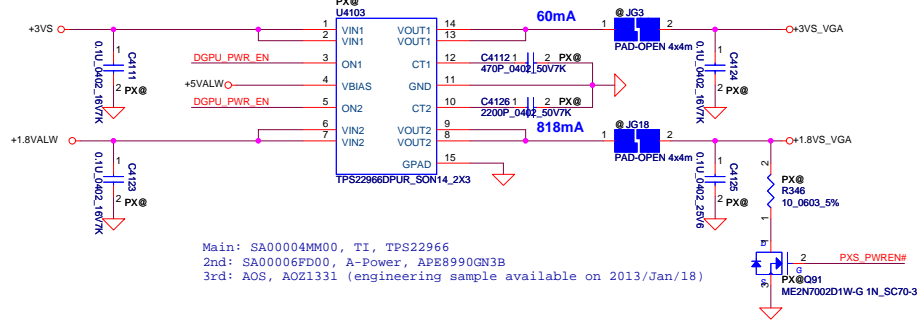
+1.5VS to +1.5VS_VGA (2.096A)



+3VS to +3VS_VGA (25mA)

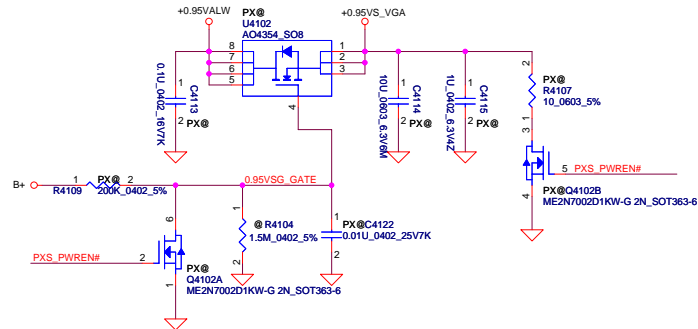
+1.8VALW to +1.8VS_VGA (311mA)

+1.8VS_VGA 必須比 +VGA_CORE晚起來



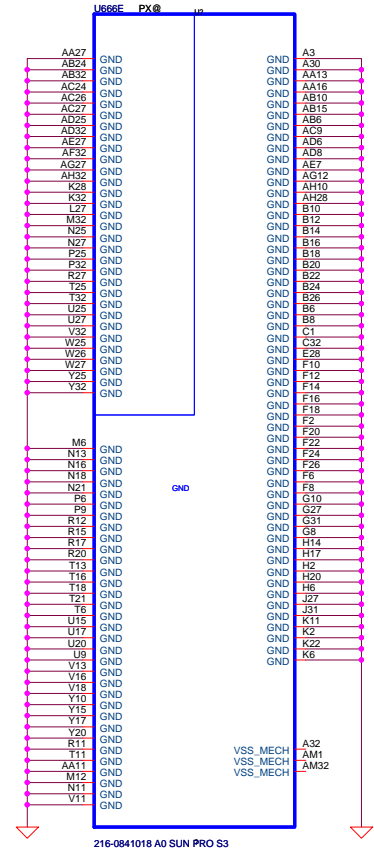
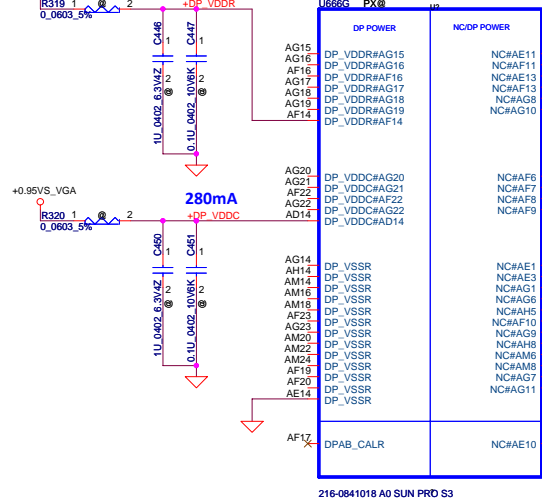
Main: SA00004MM00, TI, TPS22966
2nd: SA00006PD00, A-Power, APE8990GN3B
3rd: AOS, AOZ1331 (engineering sample available on 2013/Jan/18)

+0.95VALW to +0.95VSG (4.016A)



370mA (HDMI) 188mA (Display Port)

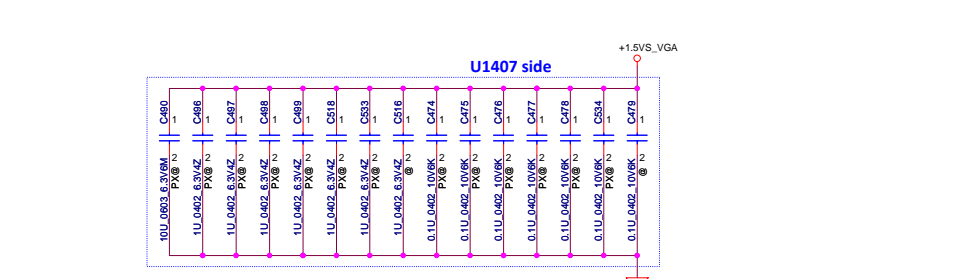
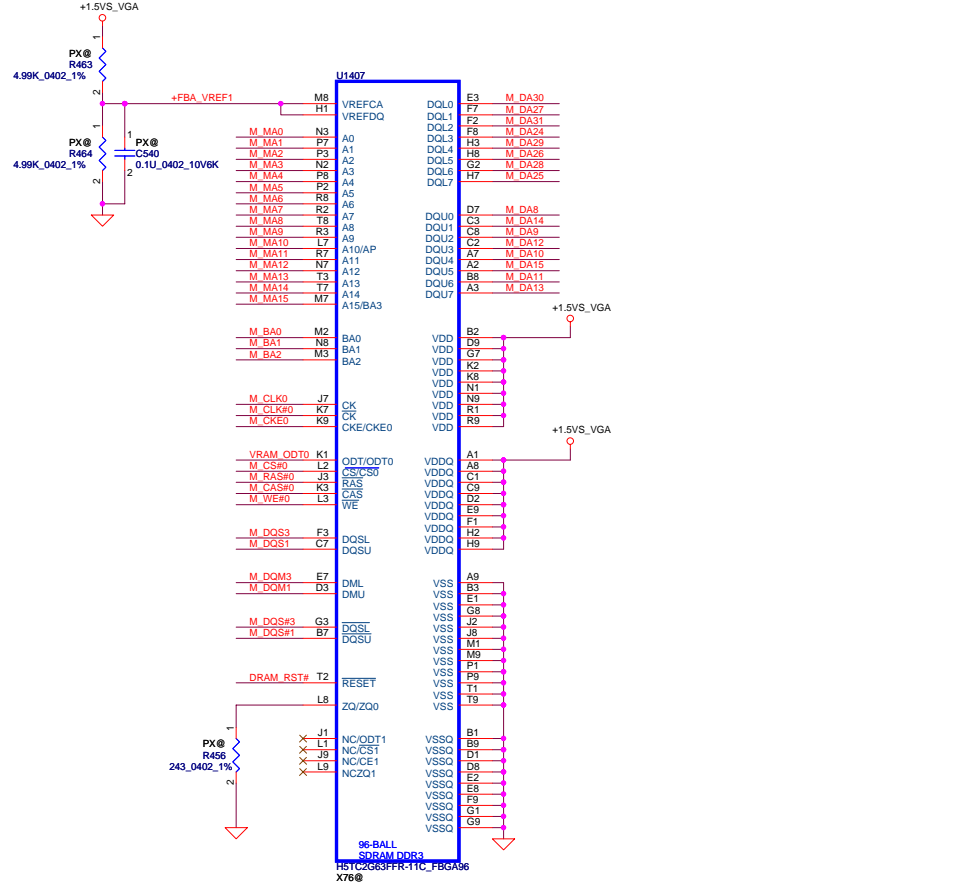
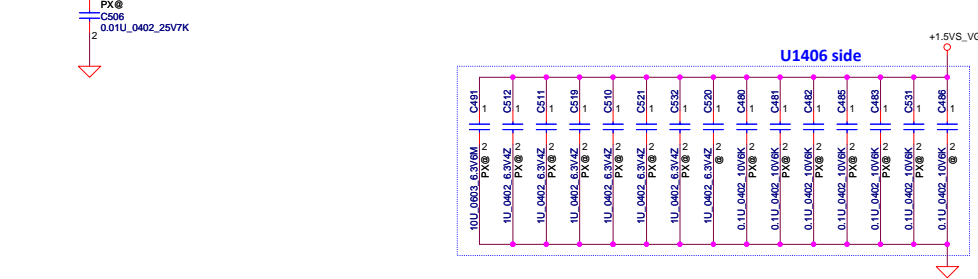
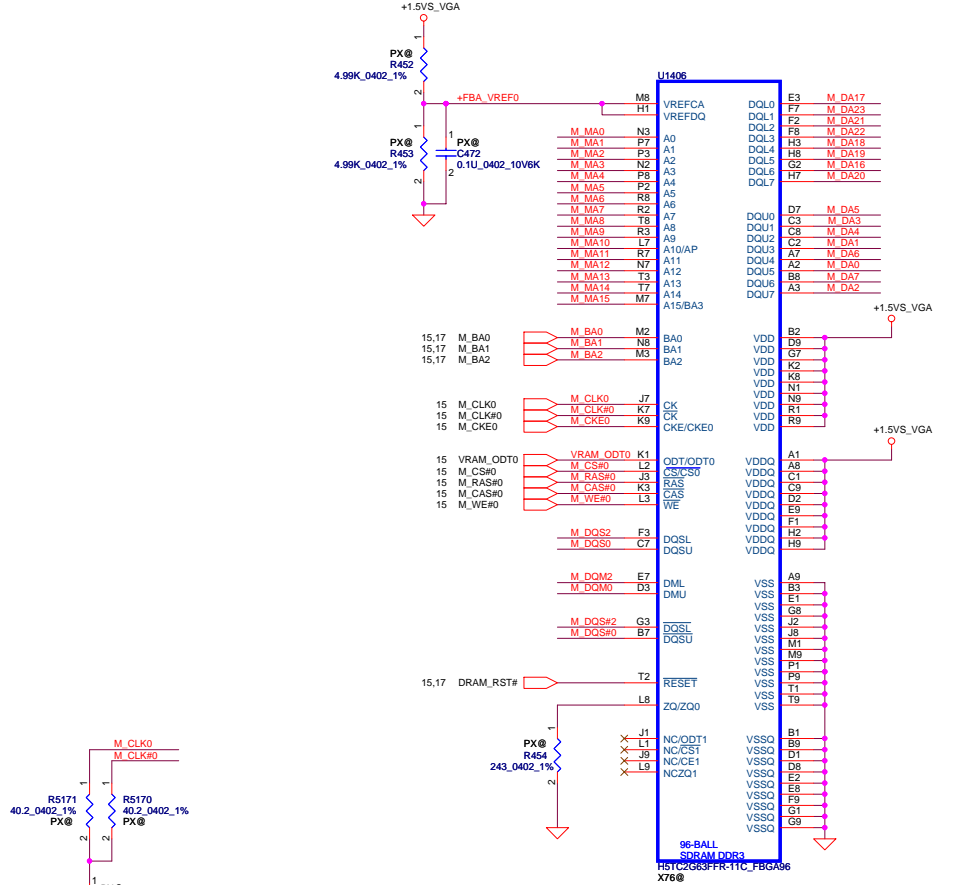
No Use GPU Display Port output



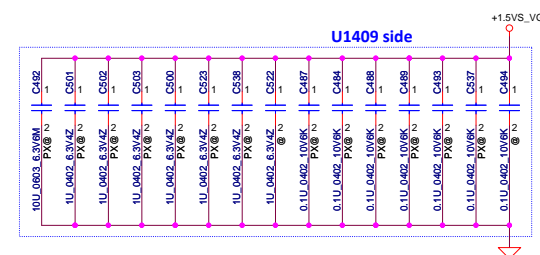
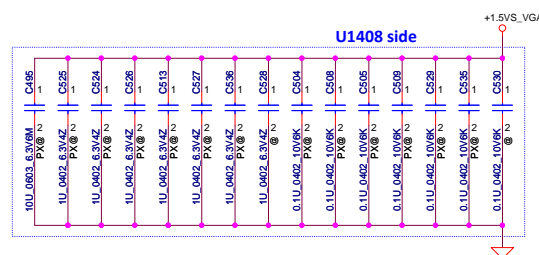
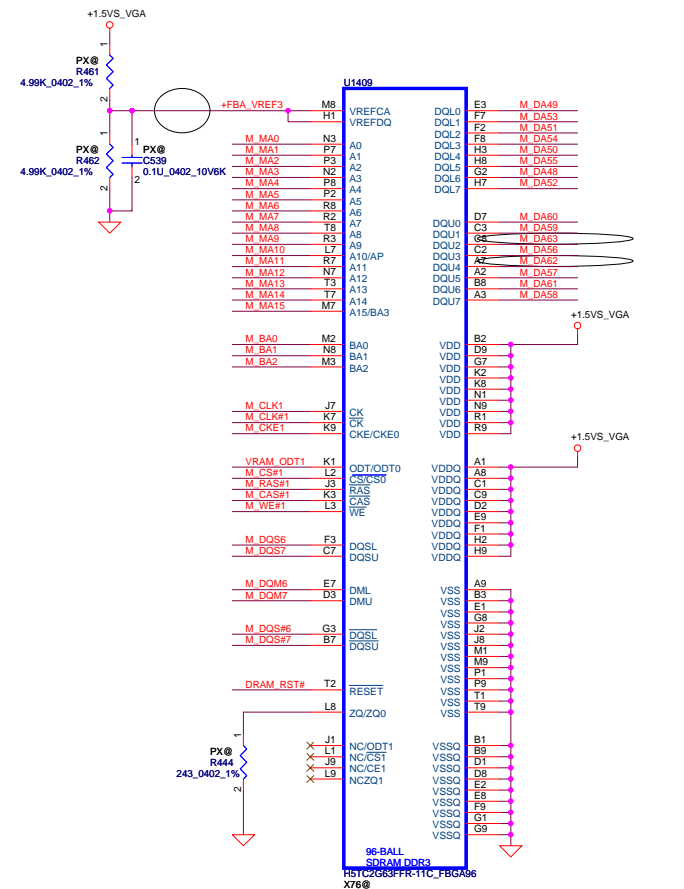
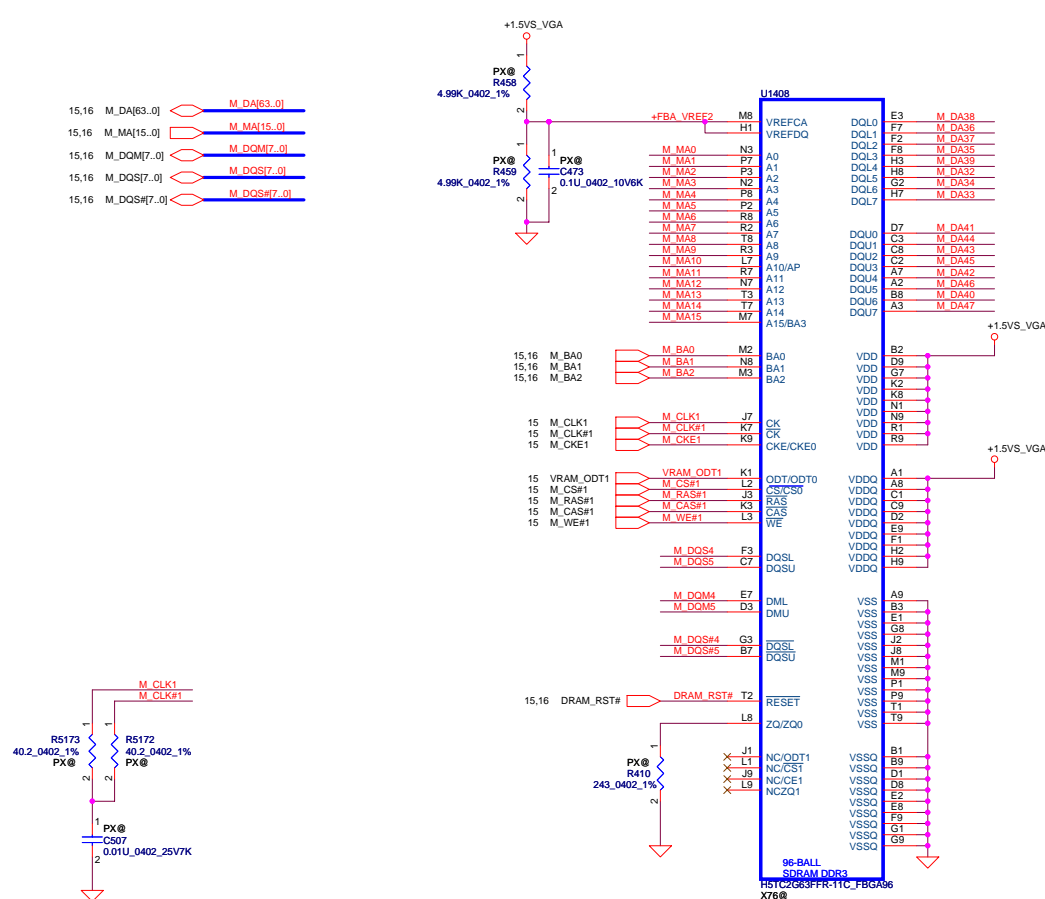
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN Power/GND
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Memory Partition A - Lower 32 bits

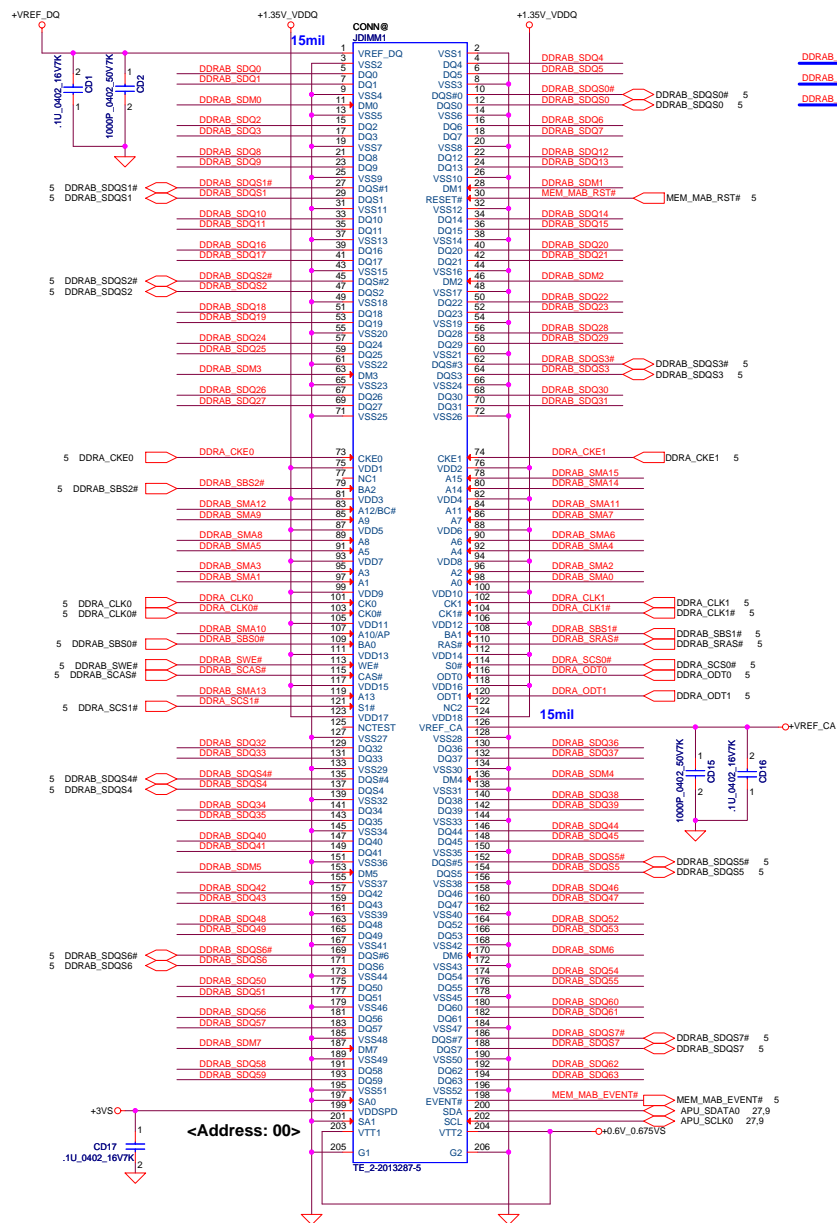
- 15.17 M_DA[63..0] M_DA[63..0]
- 15.17 M_MA[15..0] M_MA[15..0]
- 15.17 M_DQM[7..0] M_DQM[7..0]
- 15.17 M_DQS[7..0] M_DQS[7..0]
- 15.17 M_DQS# [7..0] M_DQS# [7..0]



Memory Partition A - Upper 32 bits



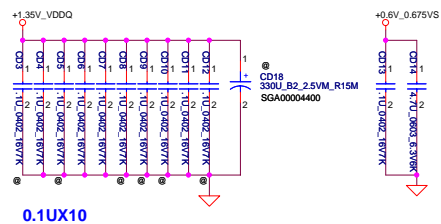
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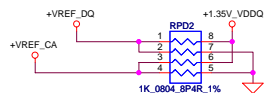
DIMM_1 H:4mm Reverse

DDRAB_SDQ[0..63] 5
DDRAB_SDM[0..7] 5
DDRAB_SMA[0..15] 5

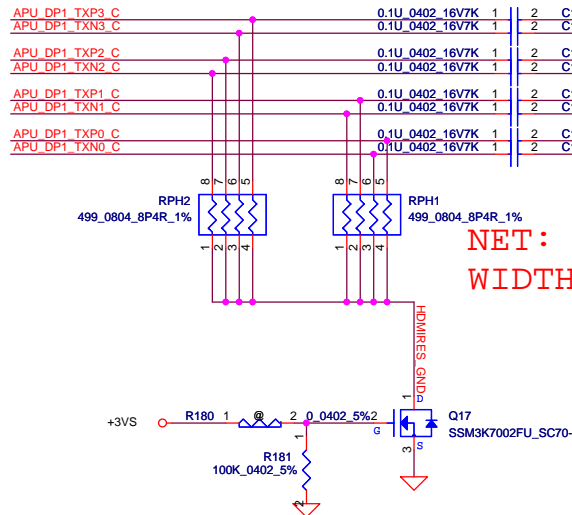
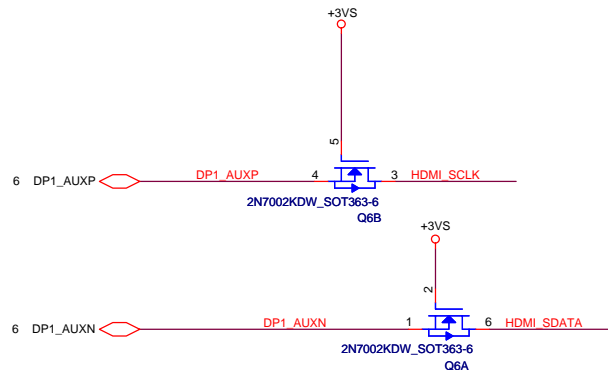
+1.35V_VDDQ/+0.675VS OF DIMM1



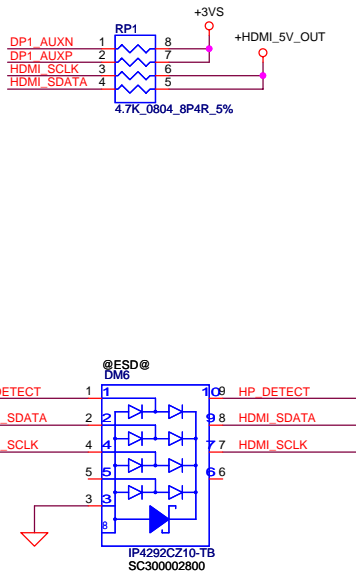
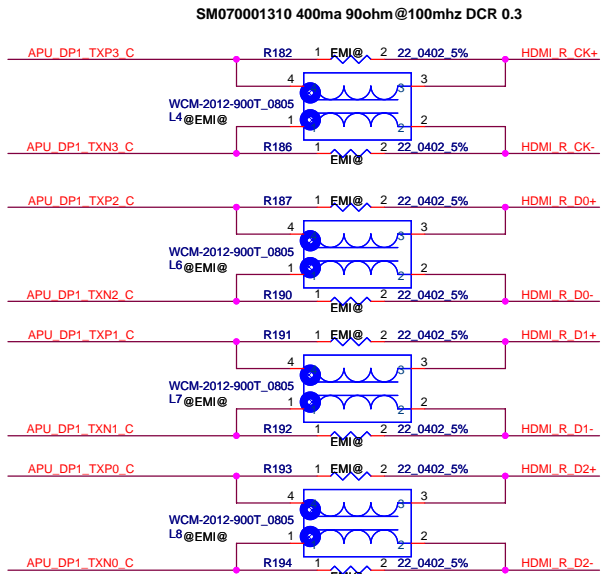
VREF for DIMM1



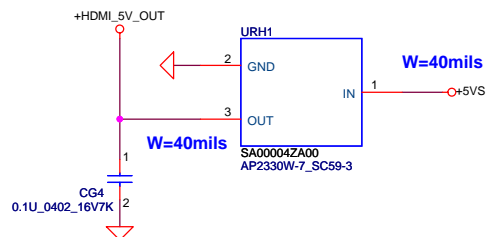
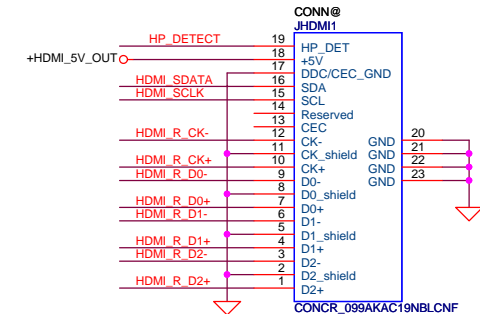
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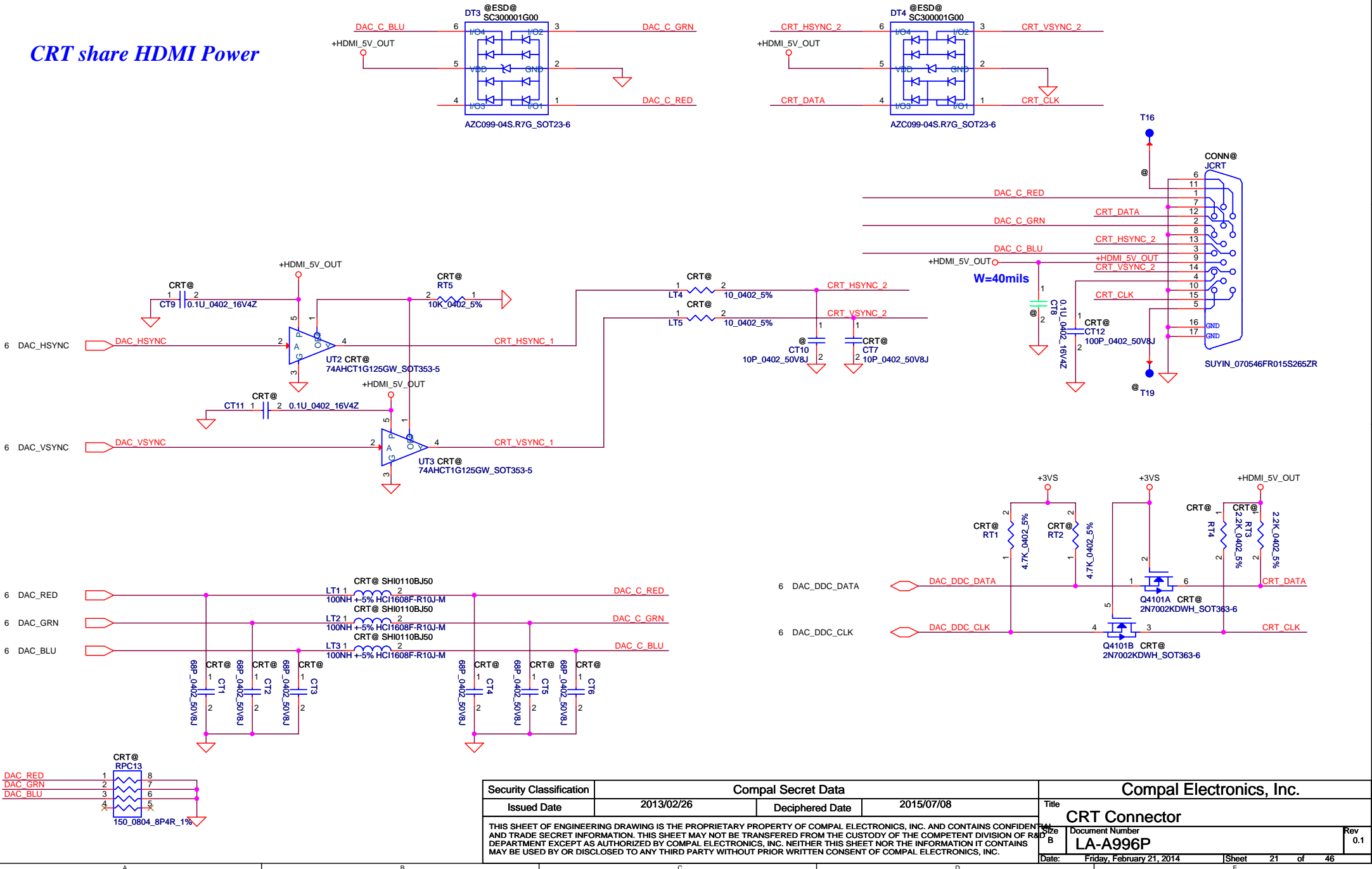


8/20 change HDMI Conn HDMI Conn.

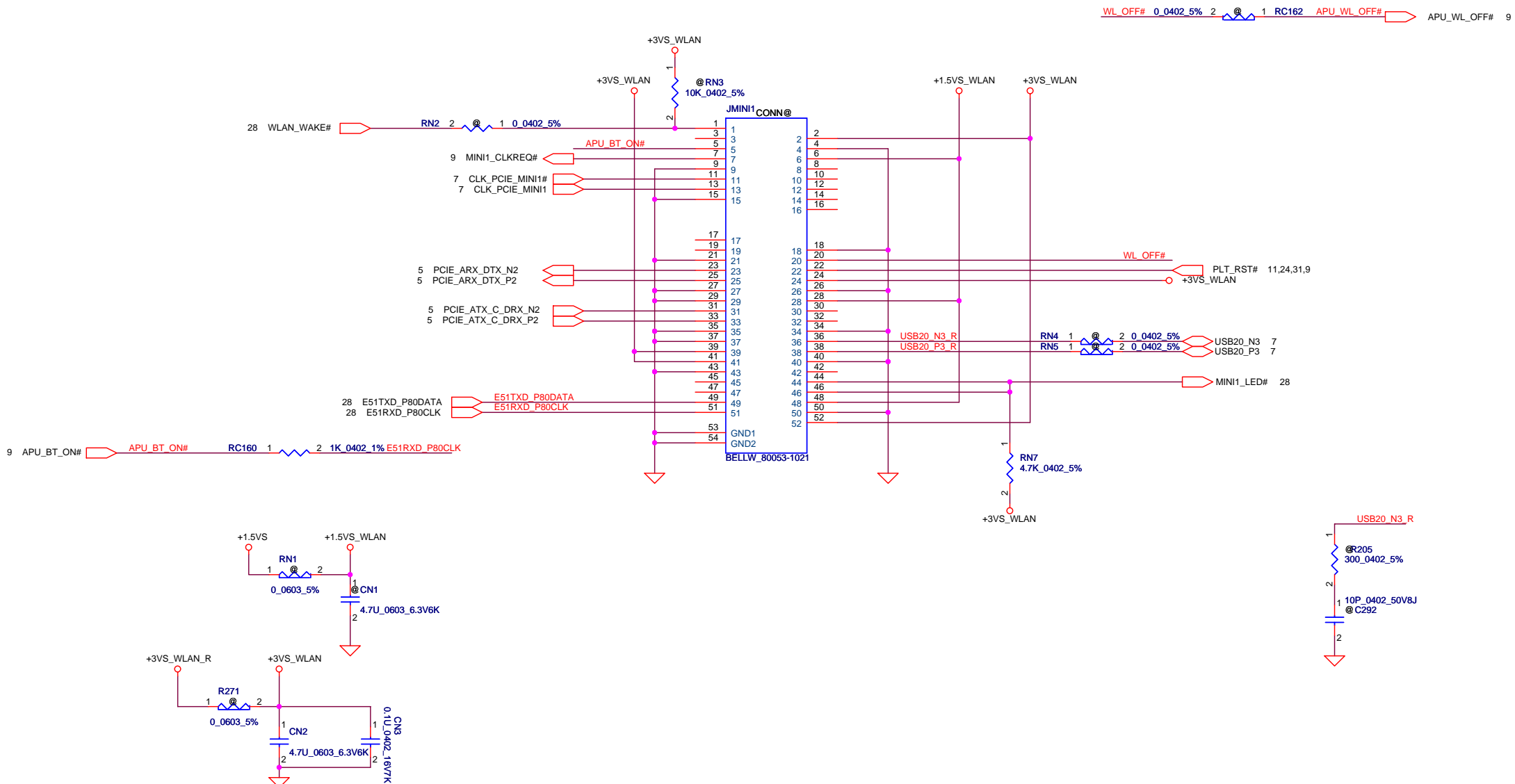


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CRT share HDMI Power

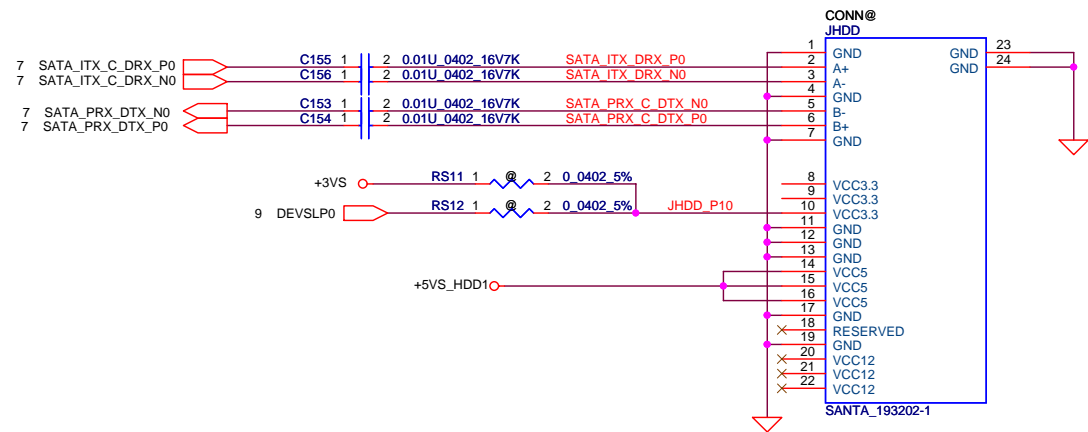
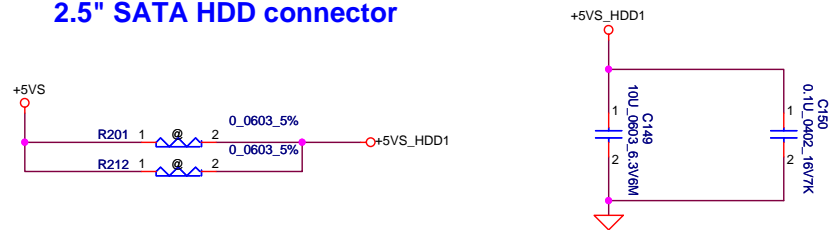


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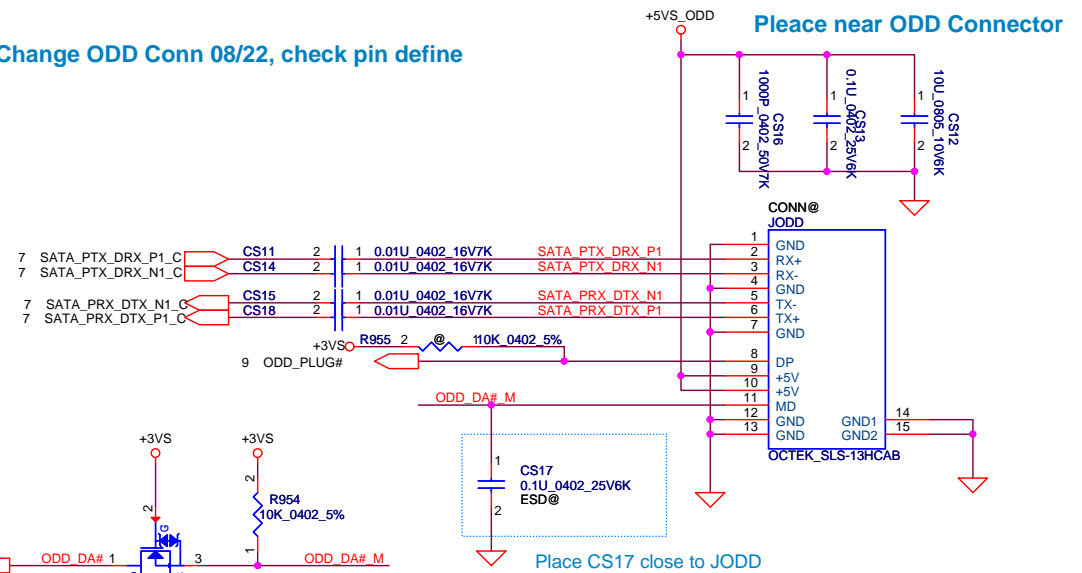
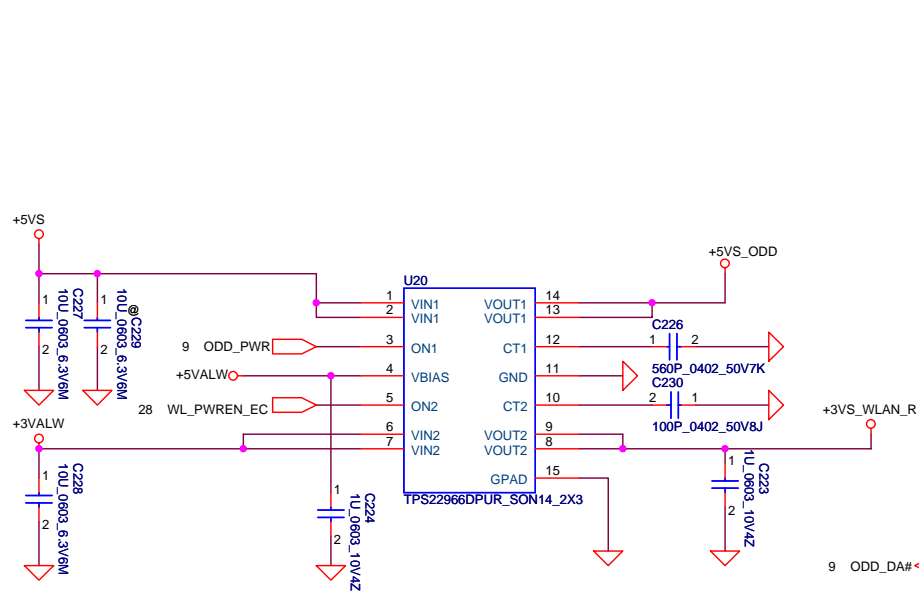


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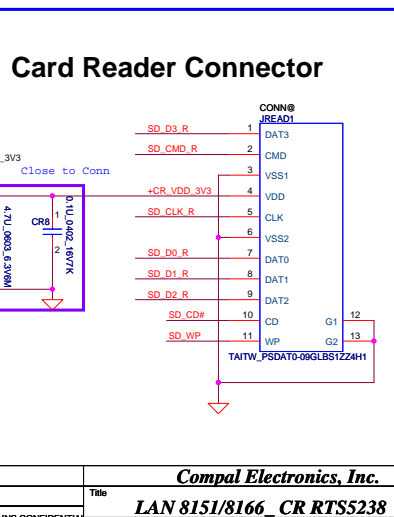
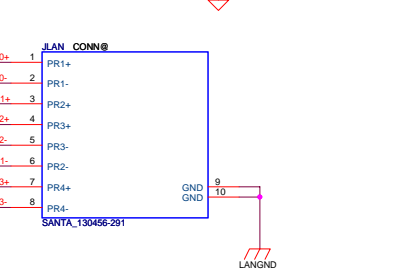
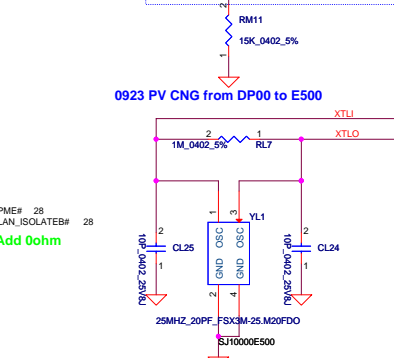
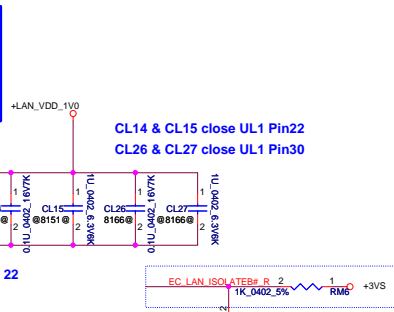
2.5" SATA HDD connector

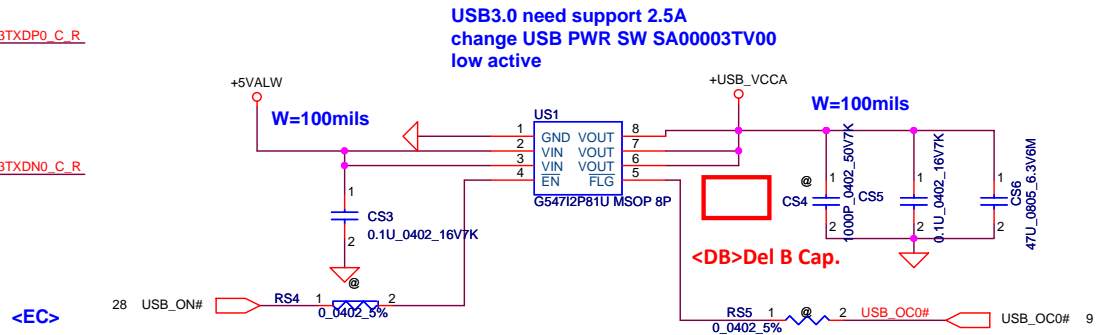
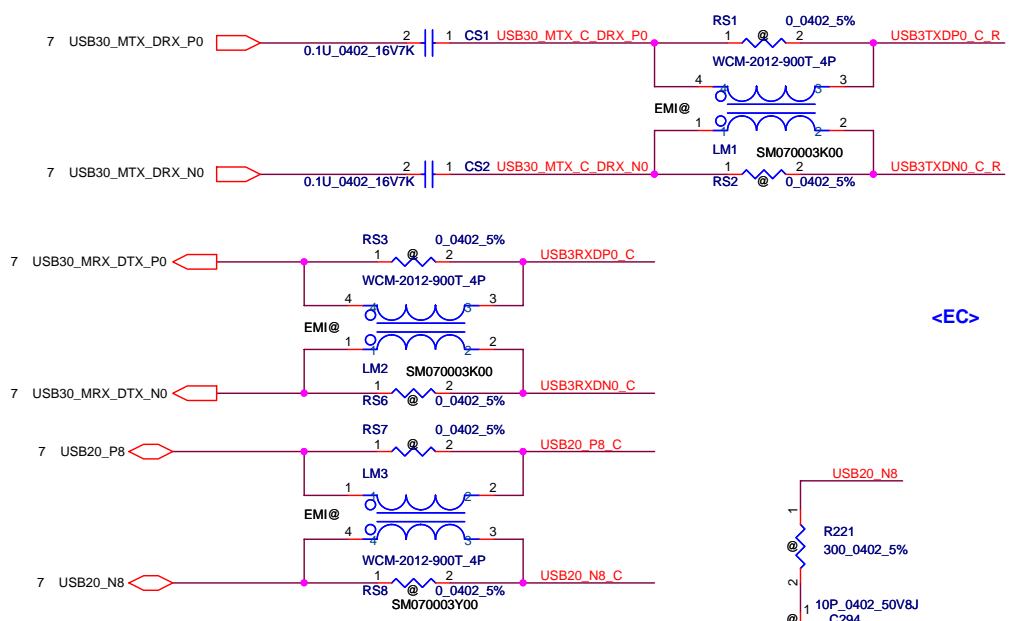


Change ODD Conn 08/22, check pin define



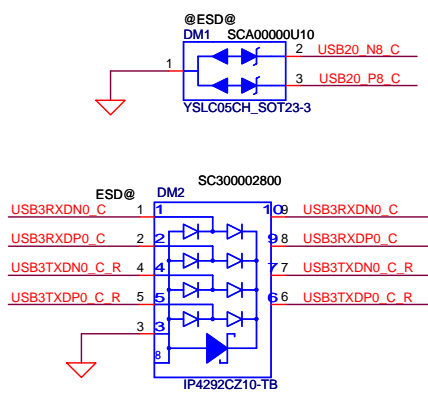
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				Date	Monday, February 17, 2014
				Sheet	23 of 46



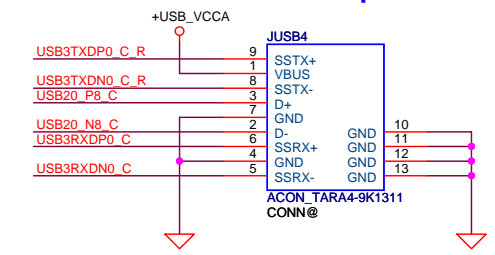


USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

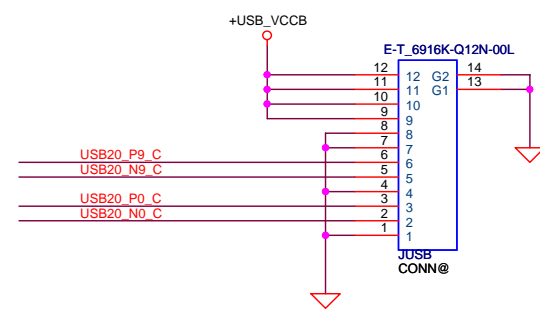
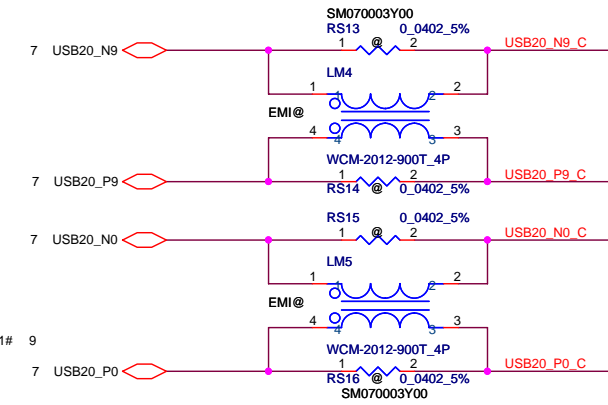
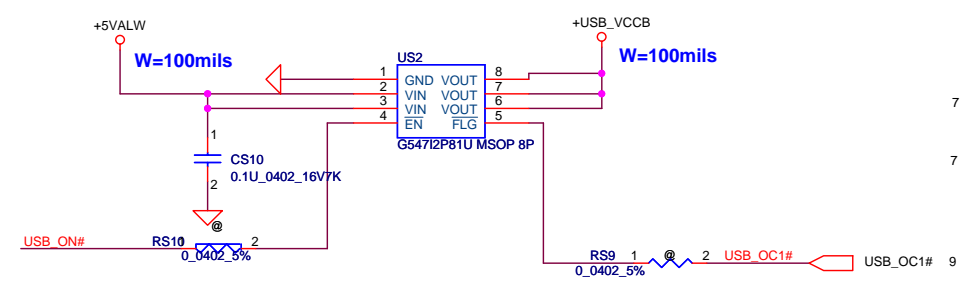
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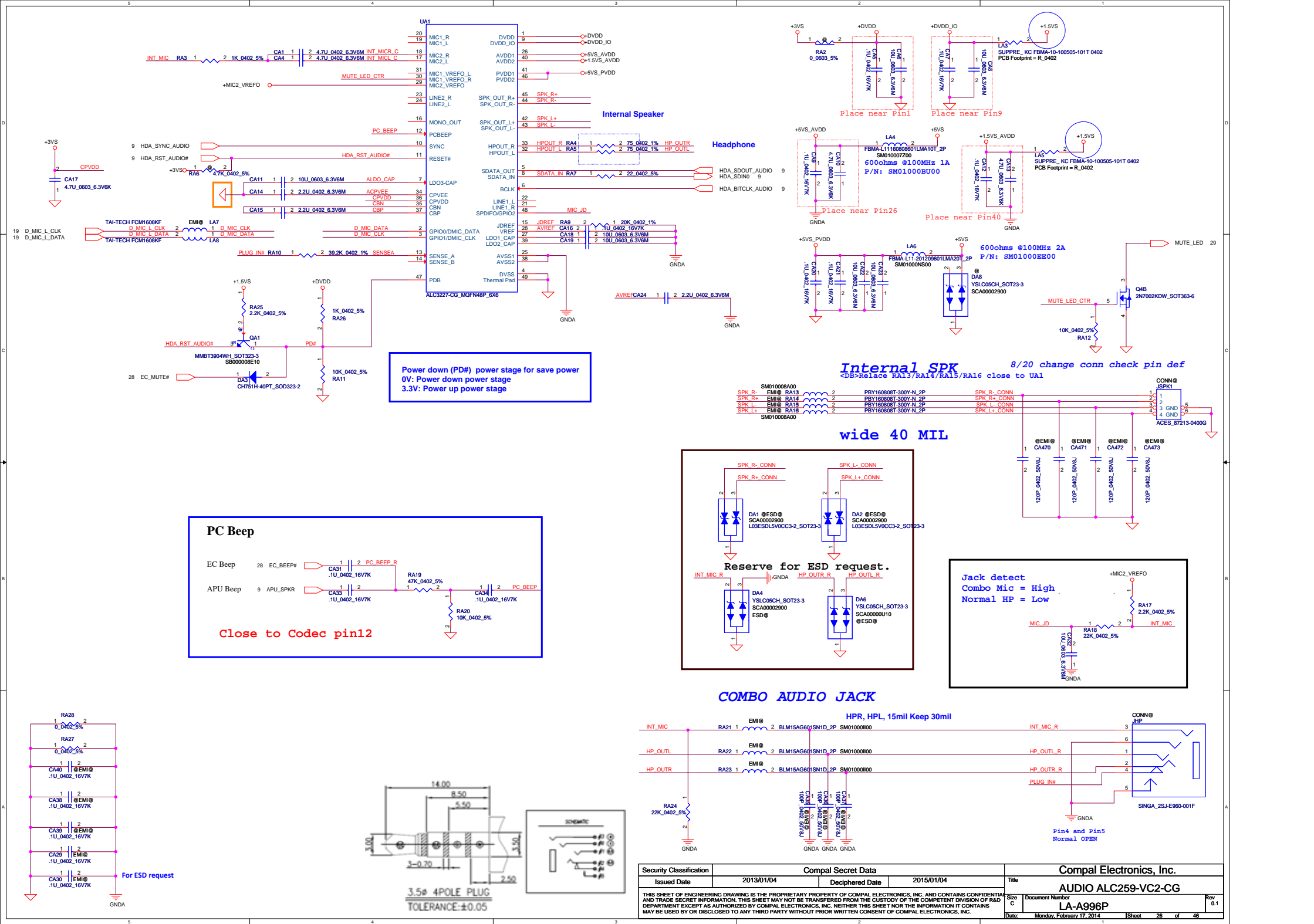
USB2.0/USB3.0 port 1

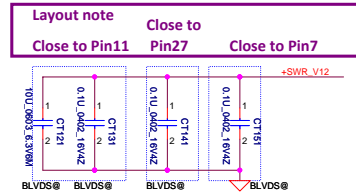
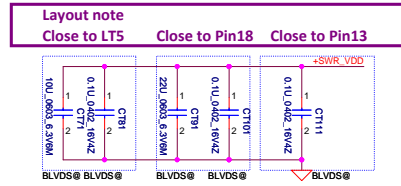
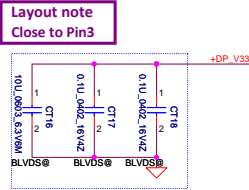
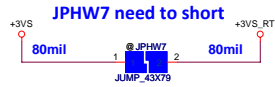


USB2.0 port x 2

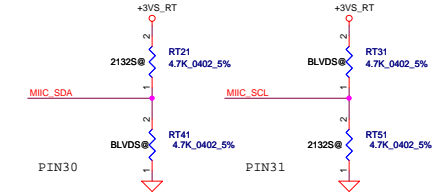


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				LA-A996P	0.1
Date: Friday, February 21, 2014				Sheet	25 of 46



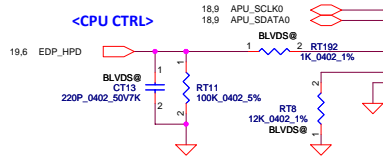
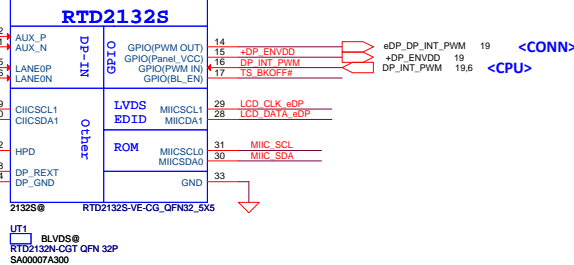
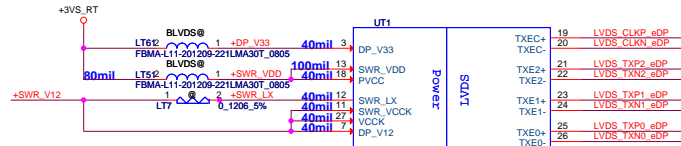


※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.
(※Default mode)

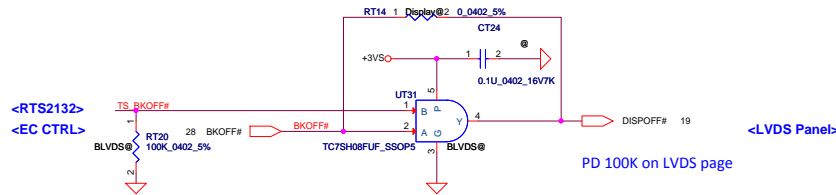


SWR / LDO Mode select		
	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

※ If use 2132N, please select LDO mode as default.



Layout note
Close to Pin8



PD 100k on LVDS page

<LVDS Panel>

LTDP0_TXP3
LTDP0_TXN3
LTDP0_TXN2

6 LVDS_CLKN
6 LVDS_CLKP
6 LVDS_TXN0
6 LVDS_TXP0

LVDS_CLKN
LVDS_CLKP
LVDS_TXN0
LVDS_TXP0

RT12 1 KLVDS@2 0.0201 5% LVDS_CLKN_F
RT13 1 KLVDS@2 0.0201 5% LVDS_CLKP_F
RT15 1 KLVDS@2 0.0201 5% LVDS_TXN0_F
RT16 1 KLVDS@2 0.0201 5% LVDS_TXP0_F

LVDS_CLKP_eDP
LVDS_CLKN_eDP
LVDS_TXP0_eDP
LVDS_TXN0_eDP

4 5
3 6
2 7
1 8

LVDS_CLKP_F
LVDS_CLKN_F
LVDS_TXP0_F
LVDS_TXN0_F

19 19
19 19
19 19
19 19

<CPU>

LTDP0_TXP1
LTDP0_TXN1

6 LVDS_TXP1
6 LVDS_TXN1

LVDS_TXP1
LVDS_TXN1

RT17 1 KLVDS@2 0.0201 5% LVDS_TXP1_F
RT18 1 KLVDS@2 0.0201 5% LVDS_TXN1_F

LVDS_TXP1_eDP
LVDS_TXN1_eDP
LVDS_TXP0_eDP
LVDS_TXN0_eDP

4 5
3 6
2 7
1 8

LVDS_TXP1_F
LVDS_TXN1_F
LVDS_TXP0_F
LVDS_TXN0_F

19 19
19 19
19 19
19 19

LTDP0_TXP2
LTDP0_TXN2

6 LVDS_TXP2
6 LVDS_TXN2

BLVDS@ CT21 1 2 1U_0402_16V7K H_EDP_TXP0_C.TL
BLVDS@ CT22 1 2 1U_0402_16V7K H_EDP_TXN0_C.TL

RT24 1 KLVDS@2 0.0402 5% LVDS_TXP2_F
RT25 1 KLVDS@2 0.0402 5% LVDS_TXN2_F

LVDS_TXP1_eDP
LVDS_TXN1_eDP
LVDS_TXP0_eDP
LVDS_TXN0_eDP

4 5
3 6
2 7
1 8

LVDS_TXP1_F
LVDS_TXN1_F
LVDS_TXP0_F
LVDS_TXN0_F

19 19
19 19
19 19
19 19

LTDP0_AUXP
LTDP0_AUXN

6 AUXP_DDC_CLK
6 AUXN_DDC_DATA

BLVDS@ CT19 1 2 1U_0402_16V7K H_EDP_AUXP_C.TL
BLVDS@ CT20 1 2 1U_0402_16V7K H_EDP_AUXN_C.TL

RT26 1 KLVDS@2 0.0402 5% LVDS_TXP2_F
RT27 1 KLVDS@2 0.0402 5% LVDS_TXN2_F

LVDS_TXP1_eDP
LVDS_TXN1_eDP
LVDS_TXP0_eDP
LVDS_TXN0_eDP

4 5
3 6
2 7
1 8

LVDS_TXP1_F
LVDS_TXN1_F
LVDS_TXP0_F
LVDS_TXN0_F

19 19
19 19
19 19
19 19

RP40 Close CPU

LVDS_TXP2
LVDS_TXN2
AUXP_DDC_CLK
AUXN_DDC_DATA

RT33 1 Display@2 0.0402 5% LVDS_TXP2_K
RT34 1 Display@2 0.0402 5% LVDS_TXN2_K
RT35 1 Display@2 0.0402 5% AUXP_DDC_CLK_K
RT36 1 Display@2 0.0402 5% AUXN_DDC_DATA_K

RT24 1 KLVDS@2 0.0402 5% LVDS_TXP2_F
RT25 1 KLVDS@2 0.0402 5% LVDS_TXN2_F
RT26 1 KLVDS@2 0.0402 5% LVDS_TXP2_F
RT27 1 KLVDS@2 0.0402 5% LVDS_TXN2_F

RT24 1 KLVDS@2 0.0402 5% LVDS_TXP2_F
RT25 1 KLVDS@2 0.0402 5% LVDS_TXN2_F
RT26 1 KLVDS@2 0.0402 5% LVDS_TXP2_F
RT27 1 KLVDS@2 0.0402 5% LVDS_TXN2_F

RT24~27 Close JLVDS conn

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2015/07/06

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Title
eDP to LVDS
Rev
0.1

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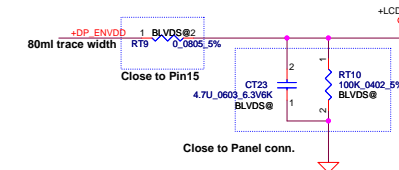
	PIN15
2132S	TL_ENVDD
BLVDS	+LCD_VDD *

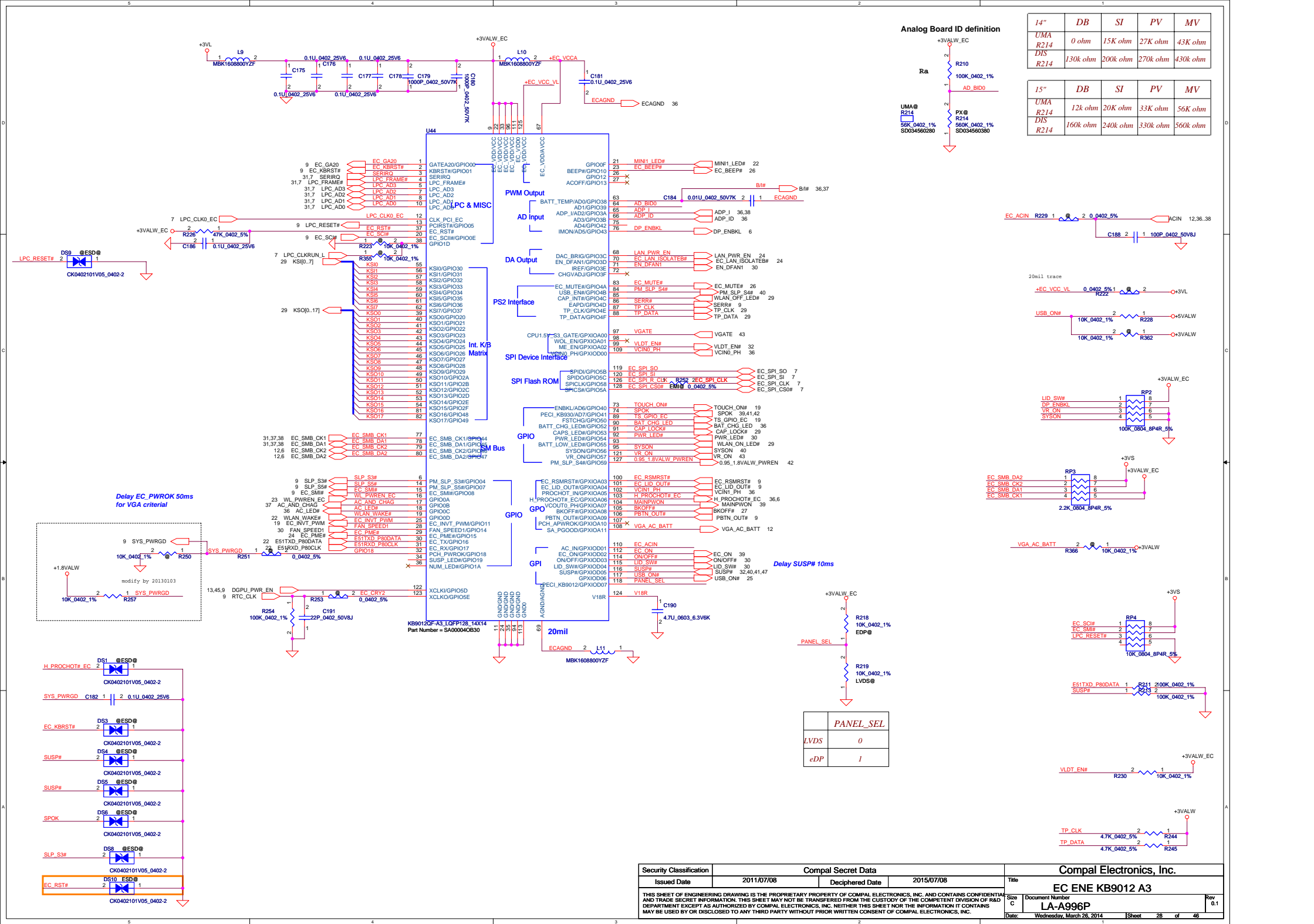
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
BLVDS	1.5~3.3V

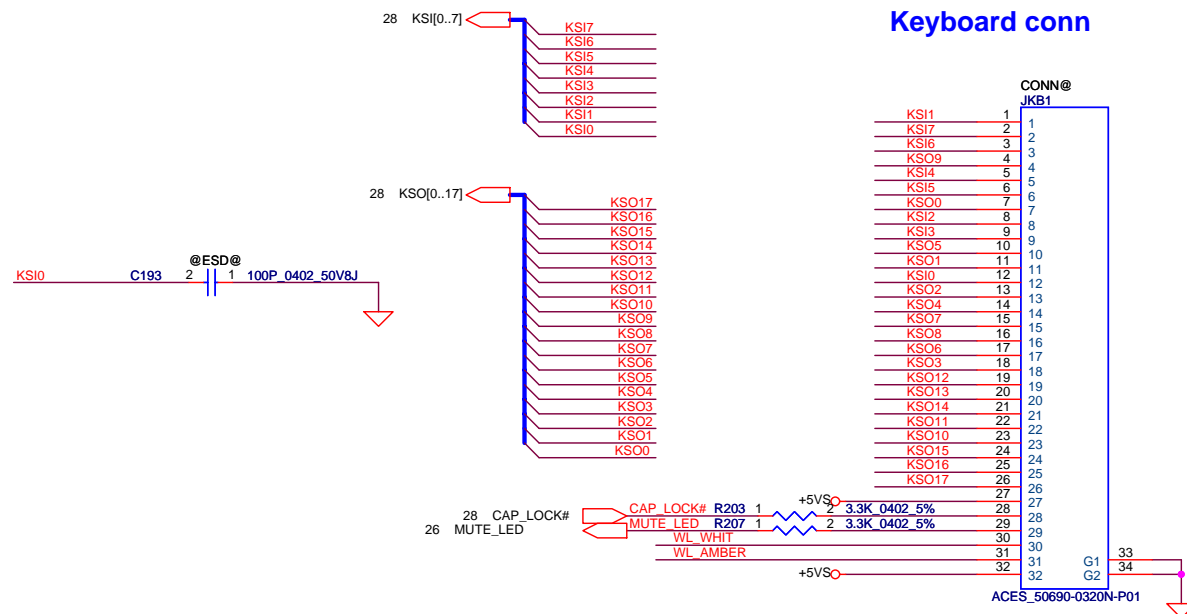
* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132N(BLVDS)	
2132S	2132N
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

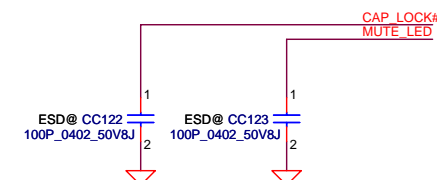
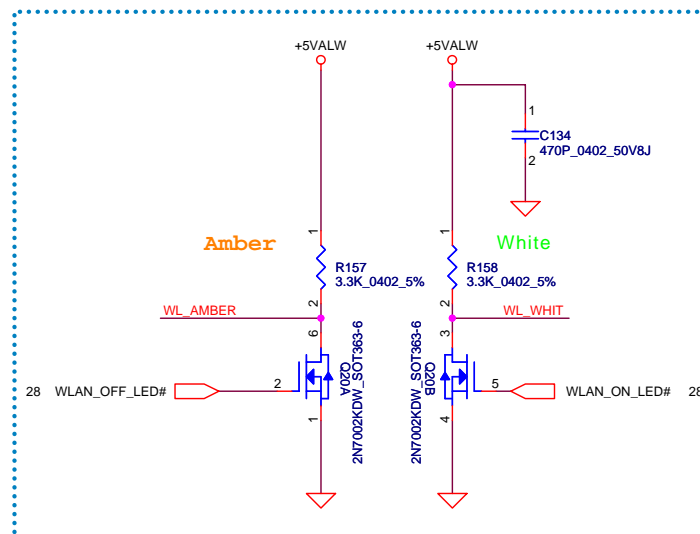
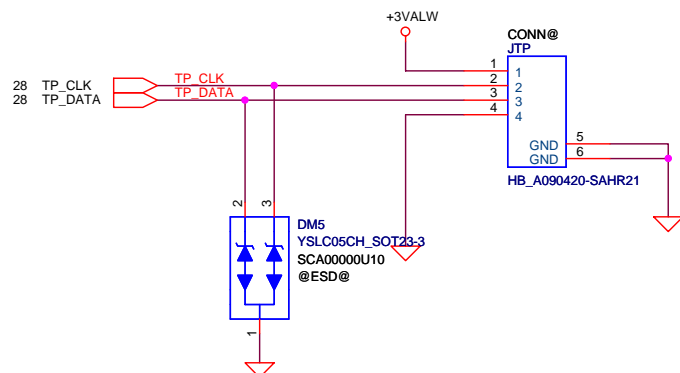




Keyboard conn

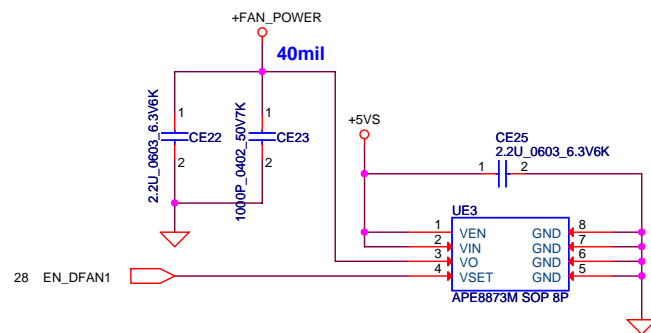
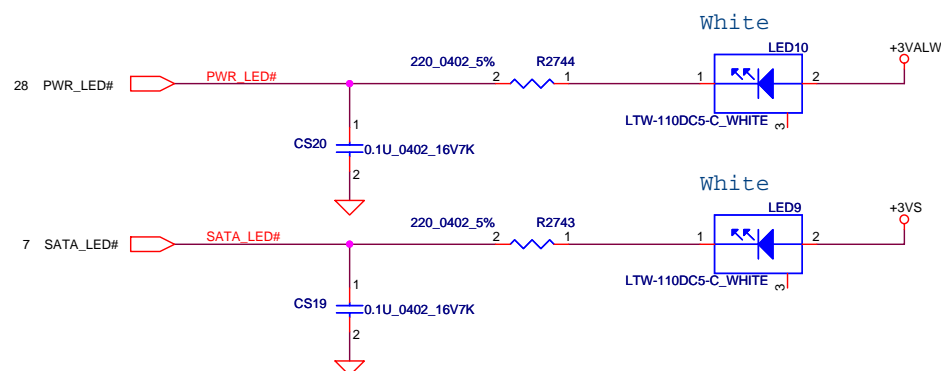
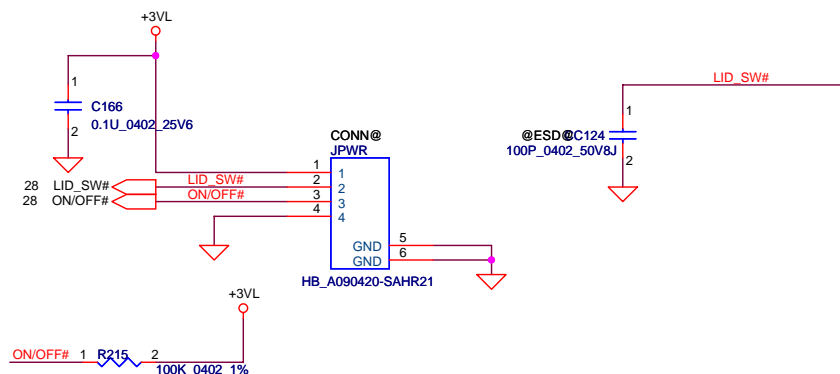


Touch pad conn

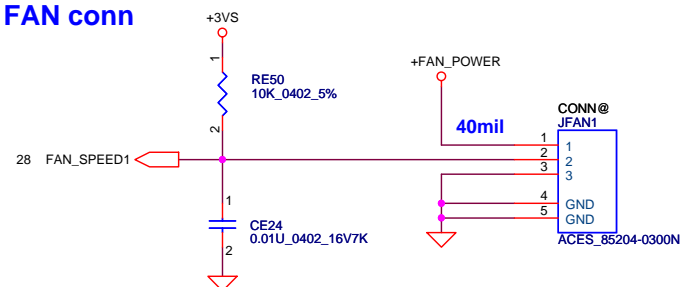


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						Document Number		LA-A996P		Rev	
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Power Button Connector

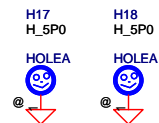
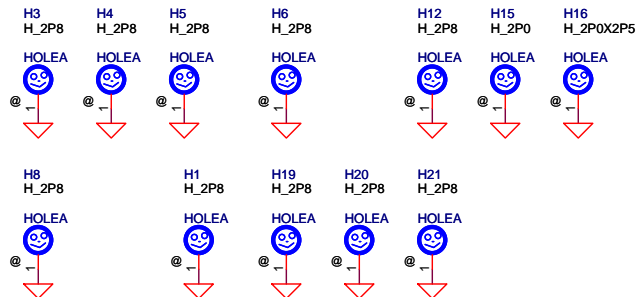
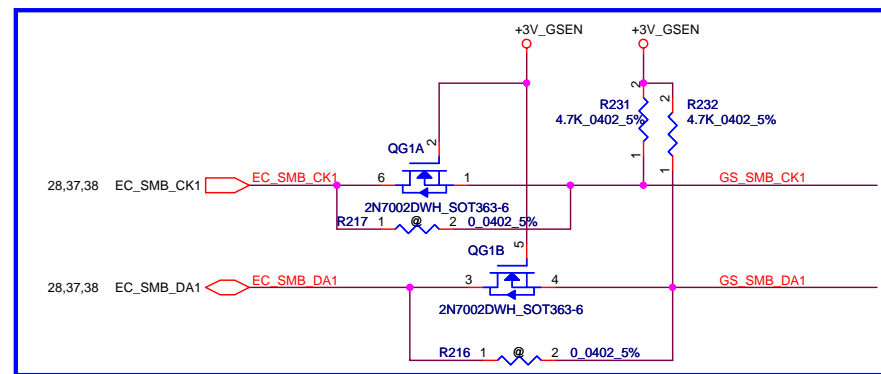
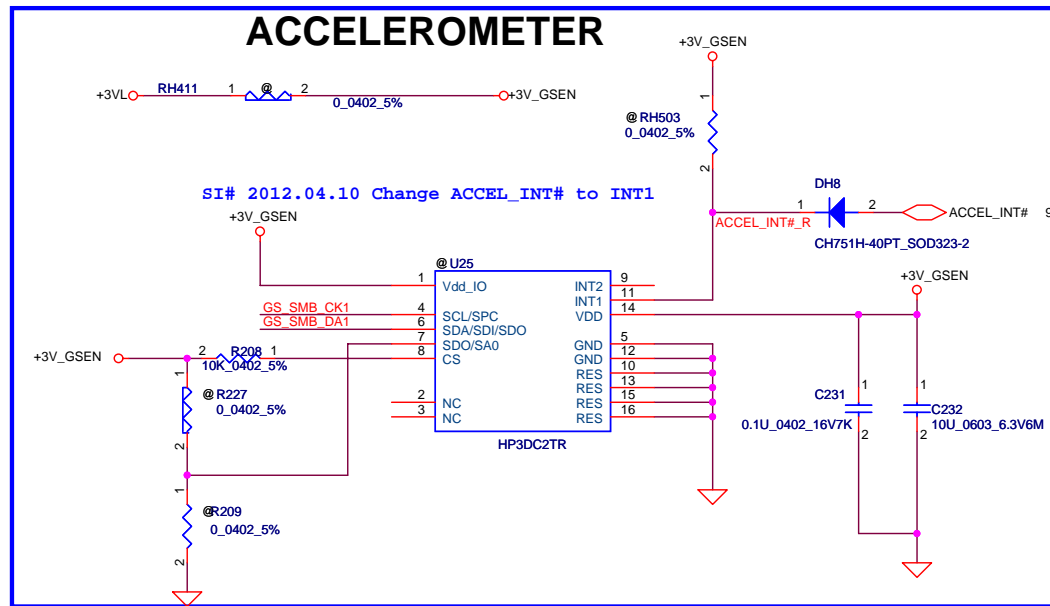


FAN conn

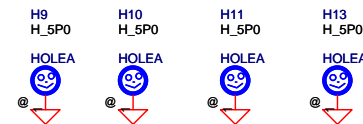


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ACCELEROMETER

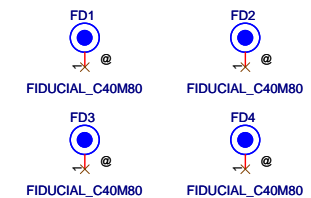
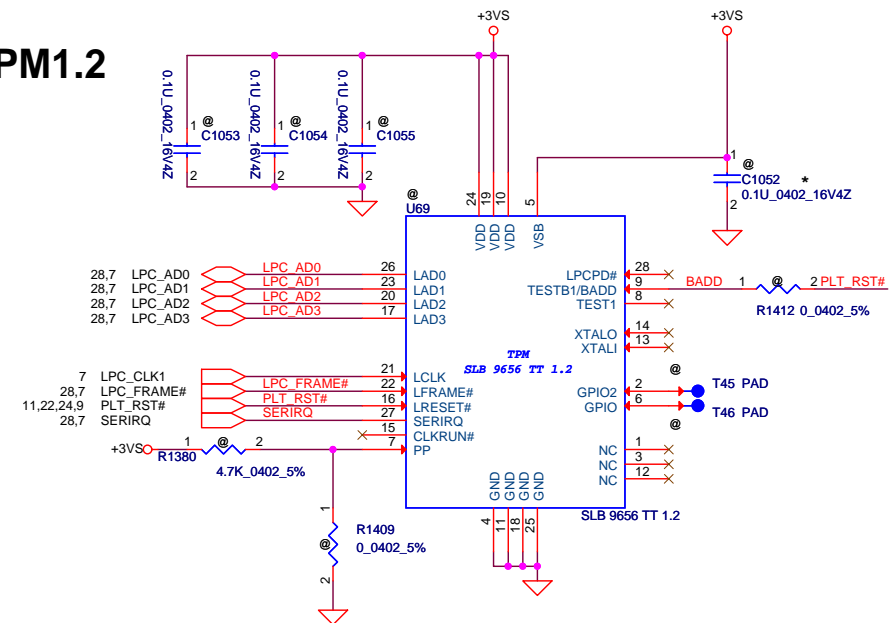


CPU

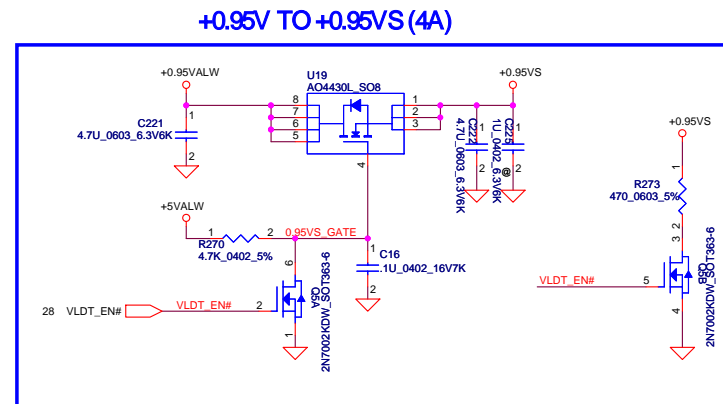
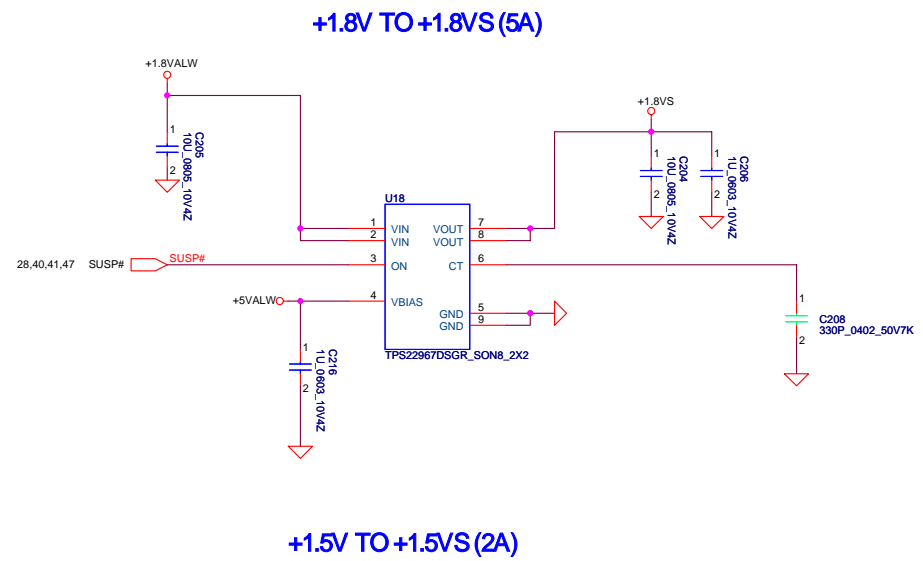
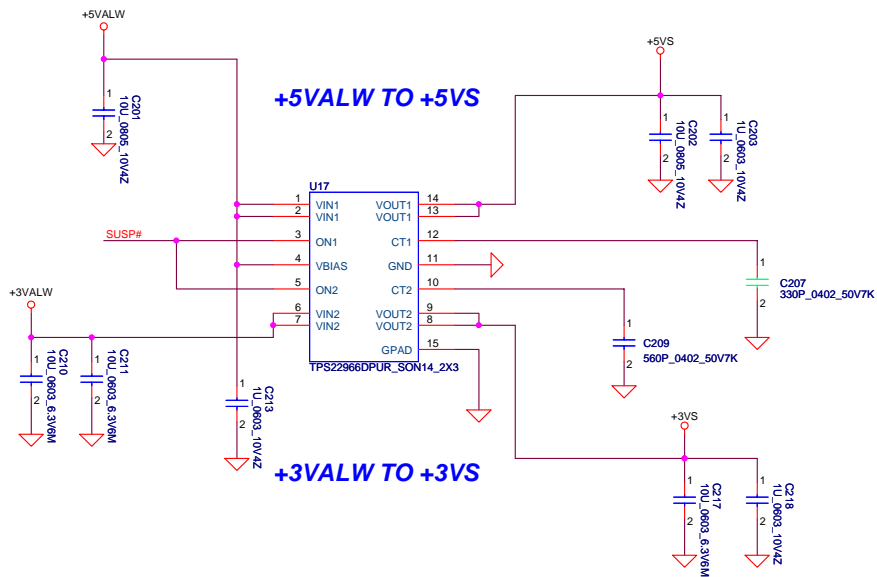


Add TPM Circuit in PV Phase

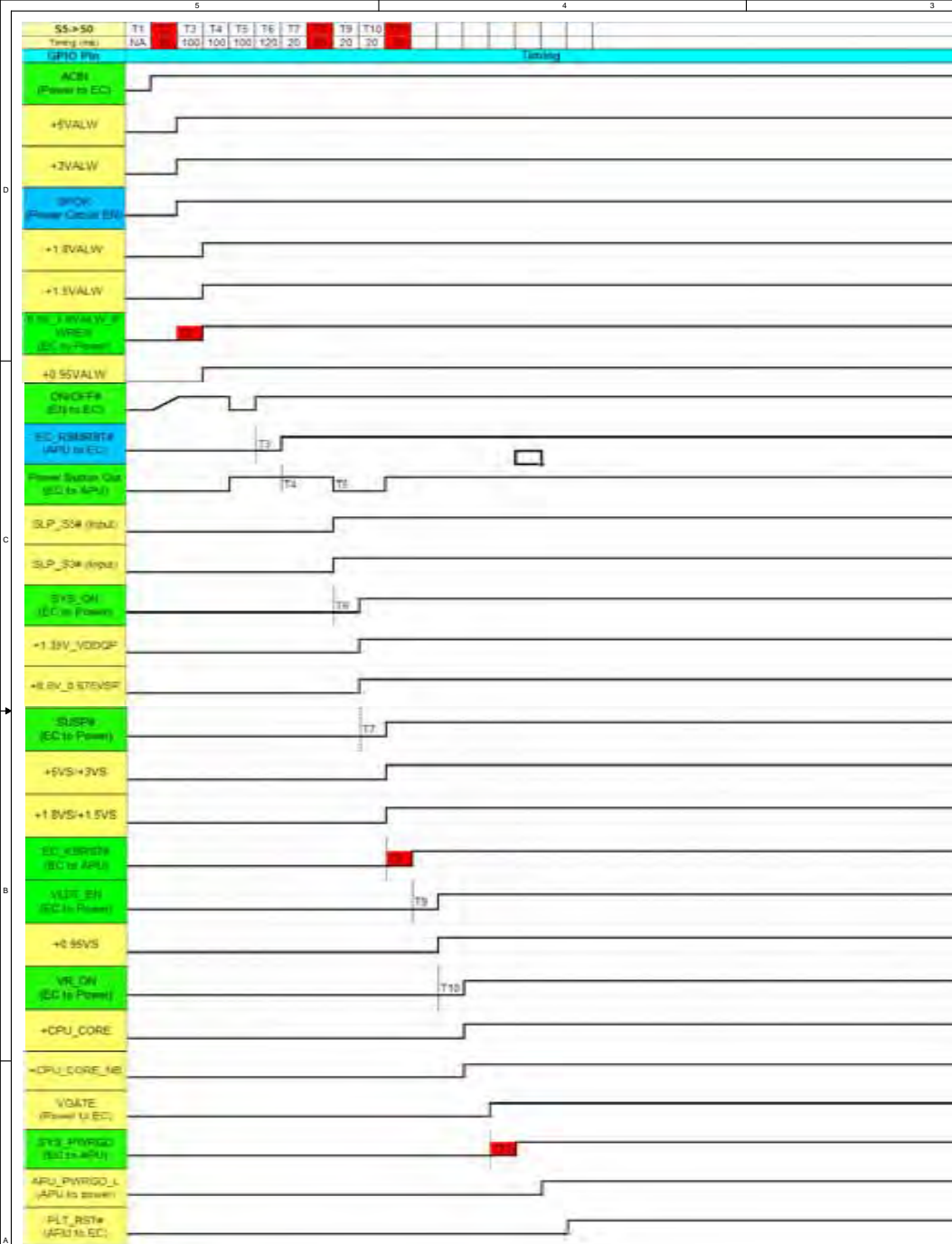
TPM1.2



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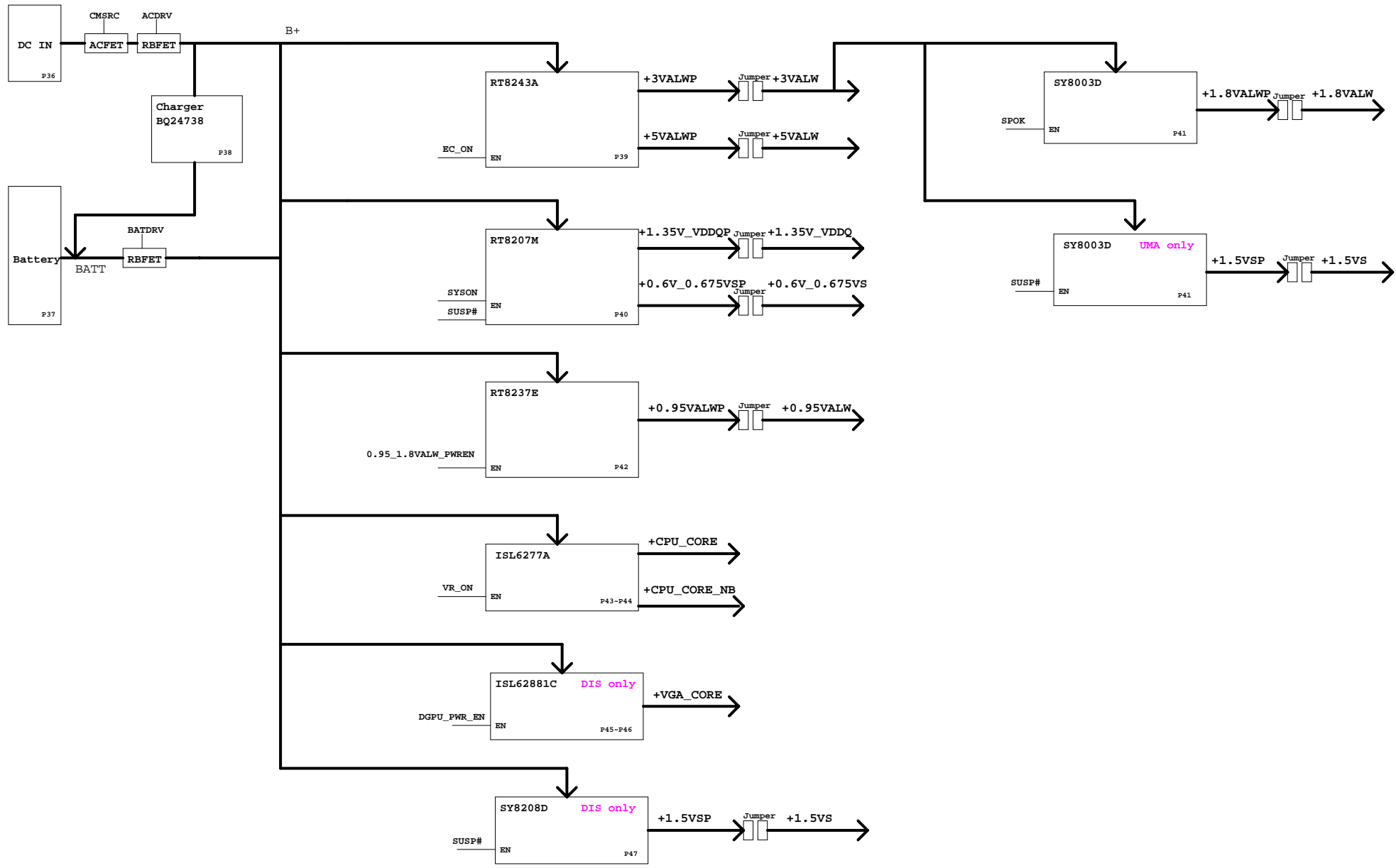
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						Document Number		Rev	
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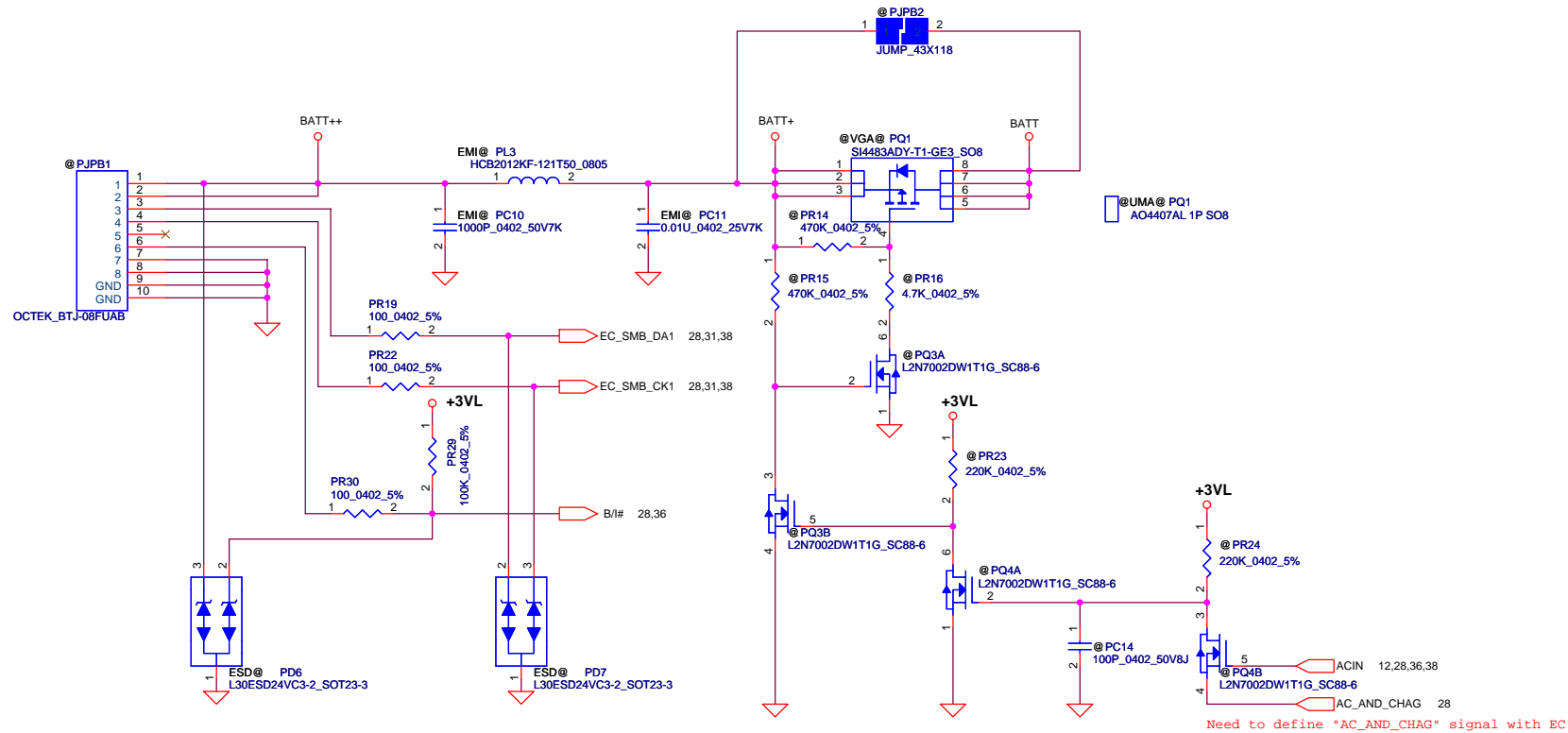
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5	4	3	2	1
D				D
C				C
B				B
A				A

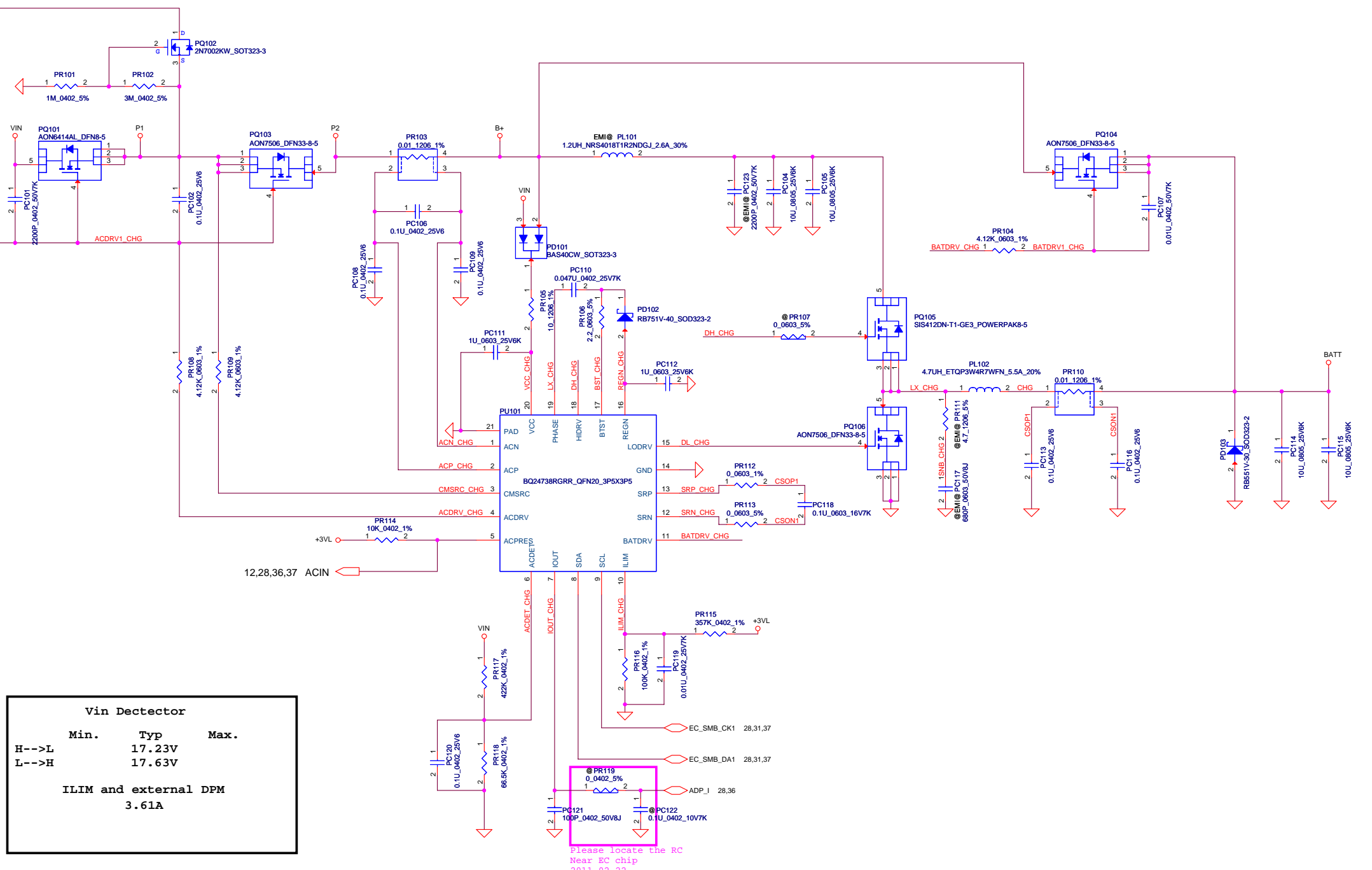
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		2014/12/31		Title	
				Power Block Diagram	
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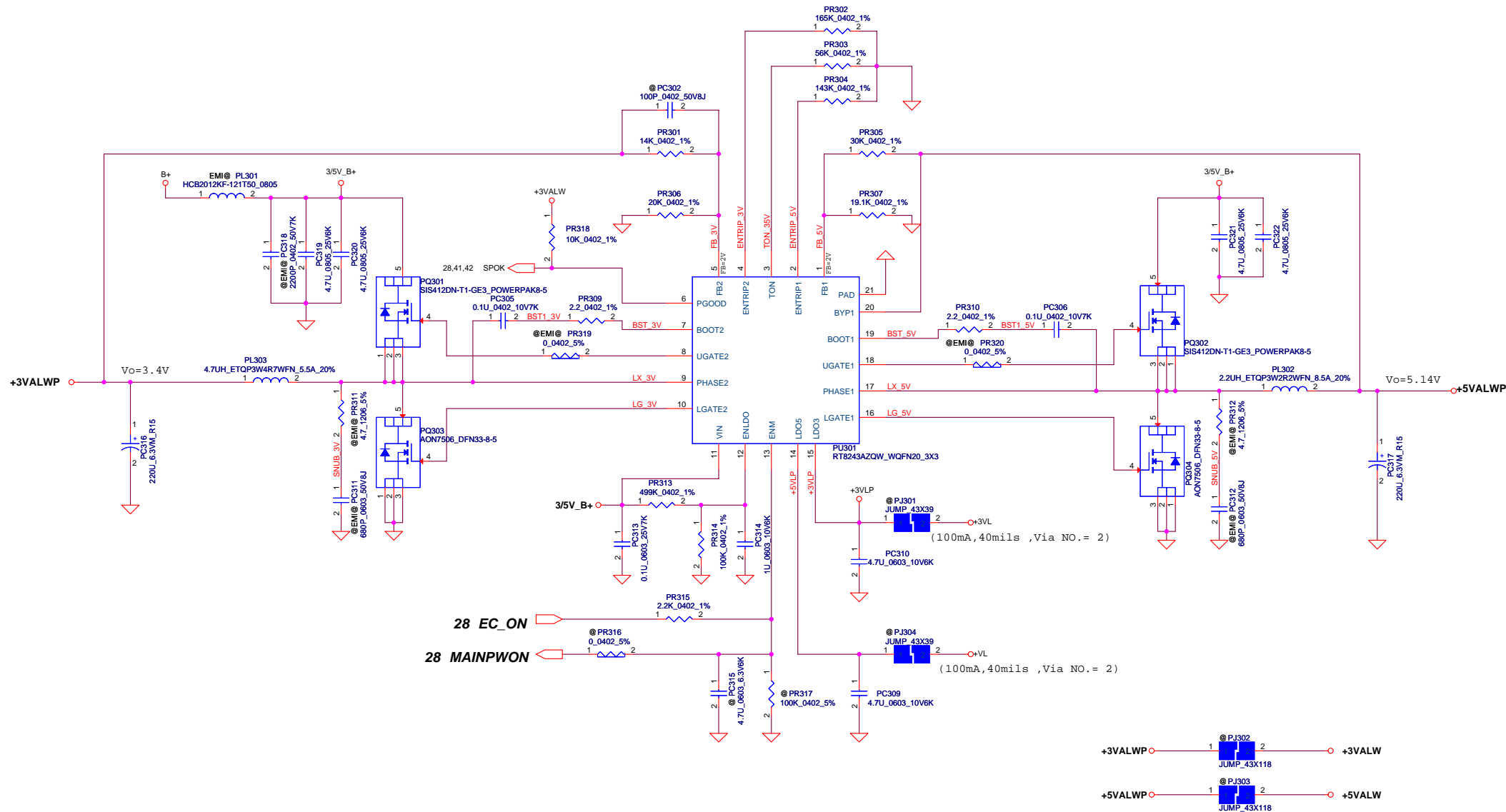


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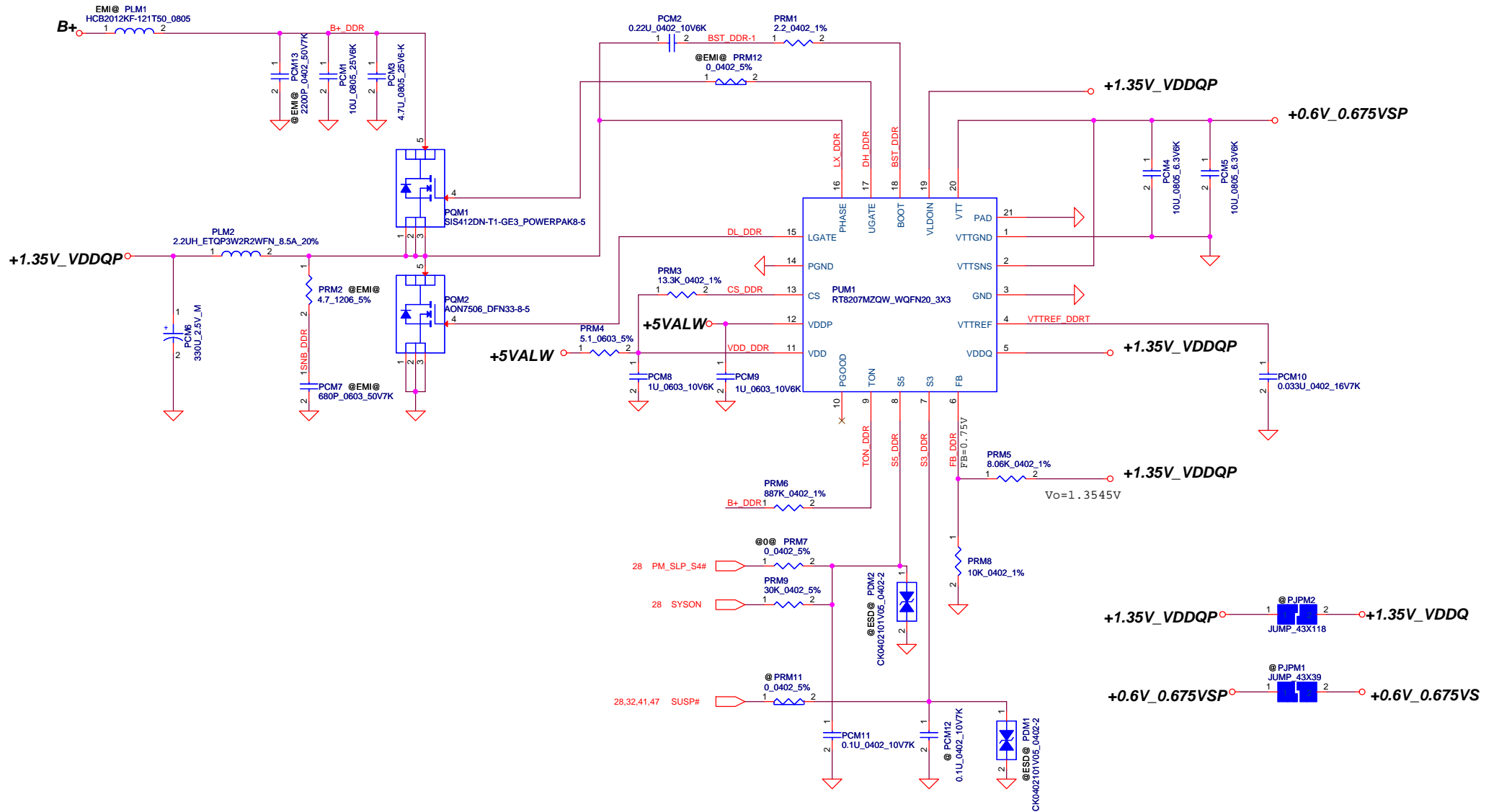


Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.61A			

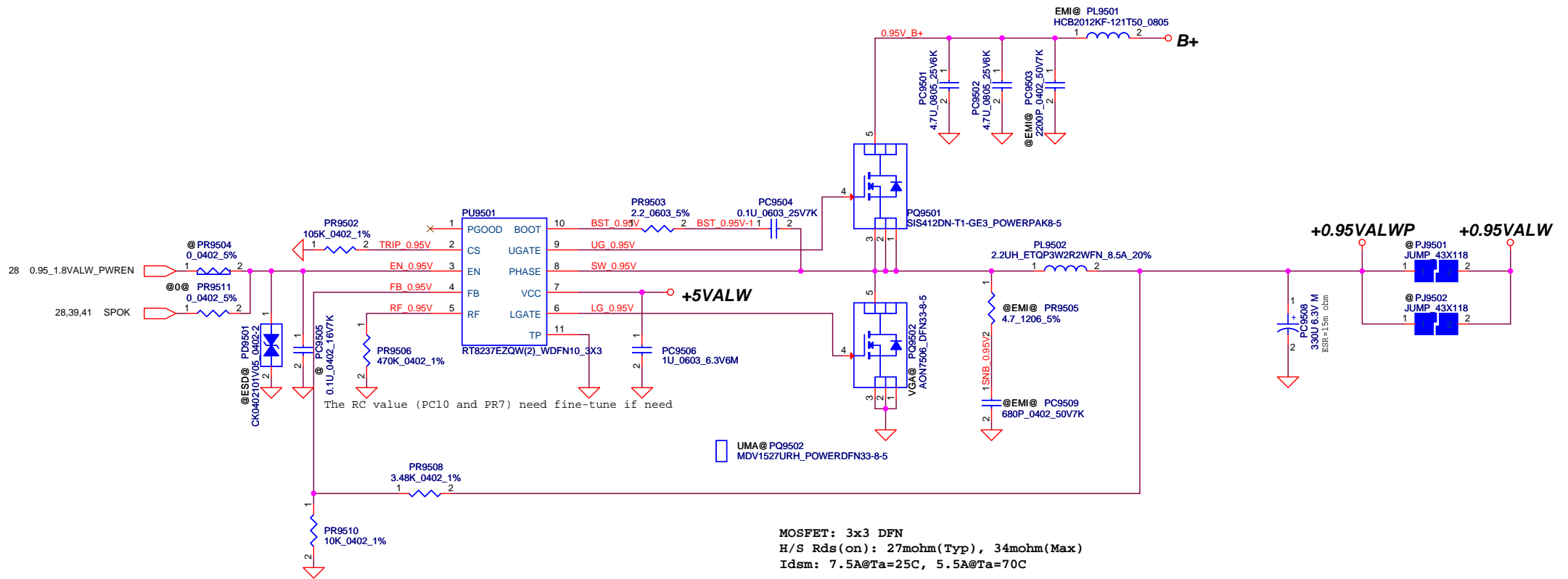
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MOSFET: 3x3 DFN
H/S $R_{ds(on)}$: 27mohm(Typ), 34mohm(Max)
 I_{dsm} : 7.5A@Ta=25C, 5.5A@Ta=70C

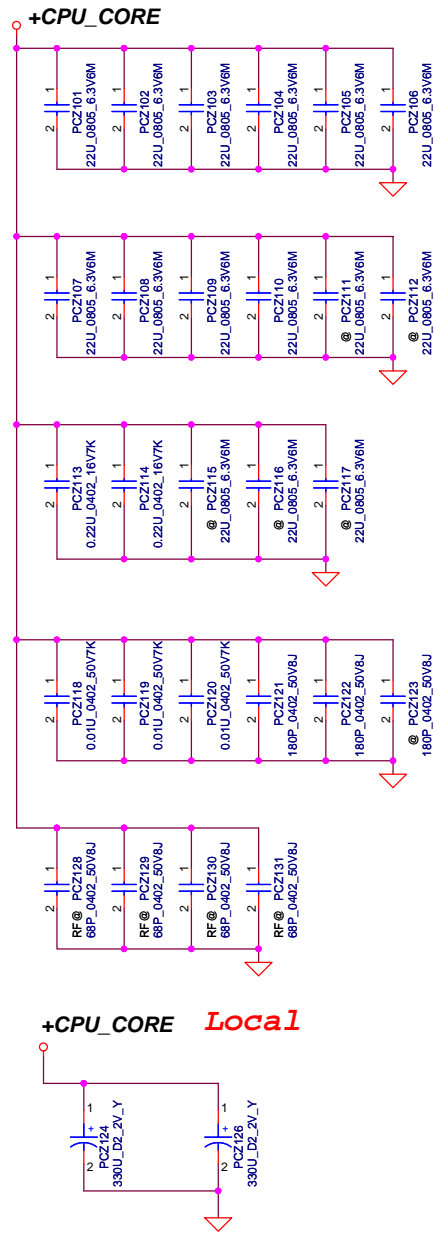
L/S $R_{ds(on)}$: 9.9mohm(Typ), 13mohm(Max)
 I_{dsm} : 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
 R_{dc} =15.5mohm +/-15%

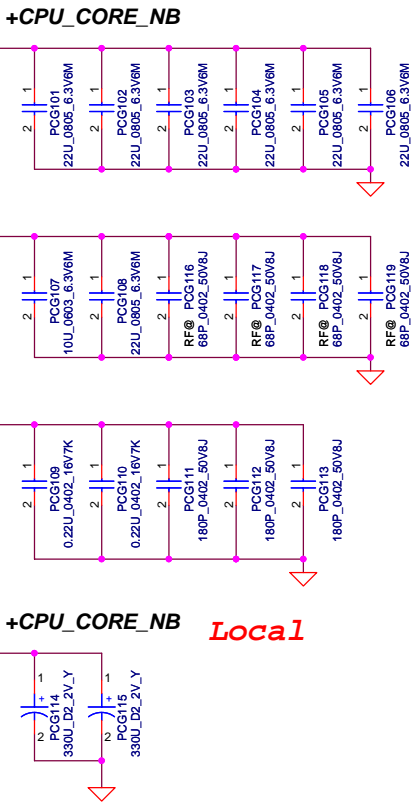
Switching Frequency: 290kHz
 I_{max} =8A
OCP~10.977A
OVP: 120%~130%
VFB=0.704V, V_{out} =0.949V
MOSFET footprint: SIS412DN

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+CPU_CORE



+CPU_CORE_NB

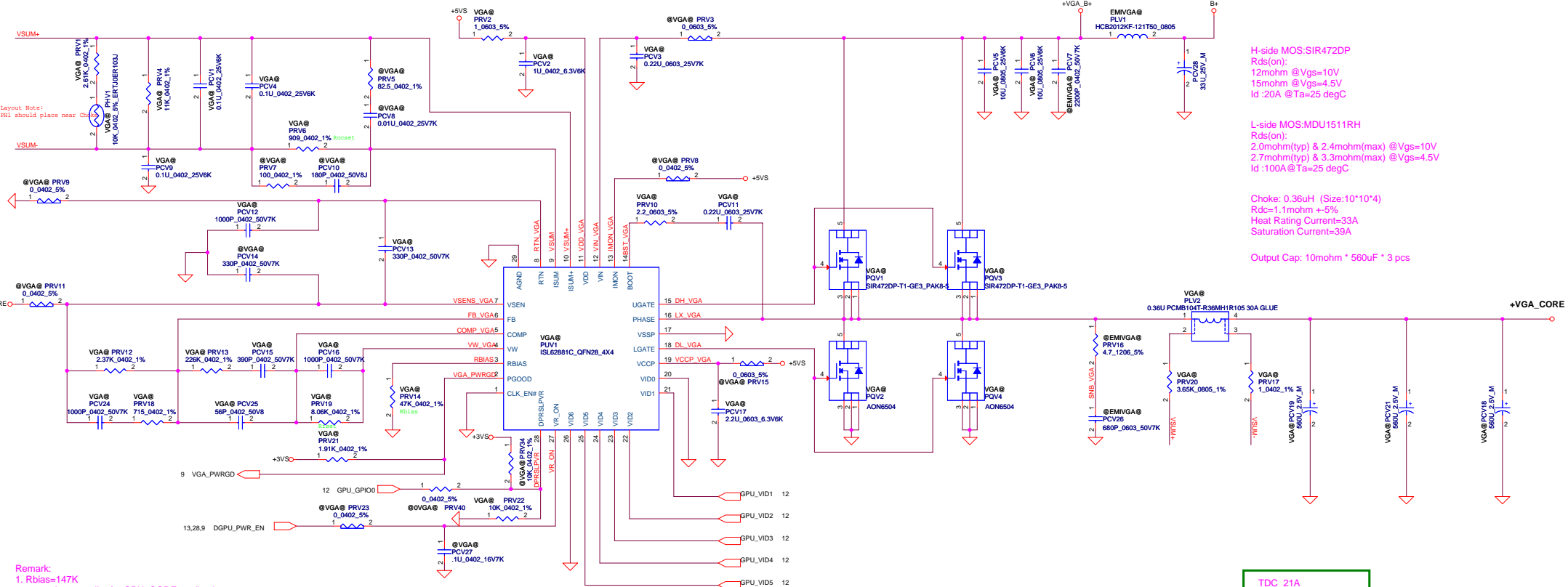


	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
+CPU_CORE	2	10	2		3	2
+CPU_CORE_NB	2	7	2	1		3

Local

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)



H-side MOS: SIR472DP
Rds(on):
12mohm @ Vgs=10V
15mohm @ Vgs=4.5V
Id :20A @ Ta=25 degC

L-side MOS: MDU1511RH
Rds(on):
2.0mohm(typ) & 2.4mohm(max) @ Vgs=10V
2.7mohm(typ) & 3.3mohm(max) @ Vgs=4.5V
Id :100A @ Ta=25 degC

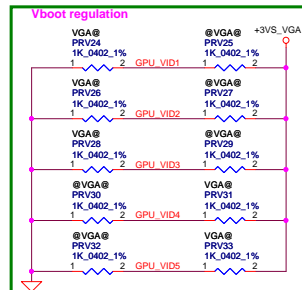
Choke: 0.36uH (Size:10*10*4)
Rds(on):
1.2mohm +5%
Heat Rating Current=33A
Saturation Current=39A

Output Cap: 10mohm * 560uF * 3 pcs

Remark:
1. Rbias=147K
=>set the controller for CPU_CORE application
Rbias=47K
=>set the controller for GPU_CORE application

2. Switching frequency setting:
Rfset(kohm)=(period(us)-0.29)*2.65
=8.06Kohm
Fsw=1/period(us)=300KHZ

3. Operation mode:
when GPU_CORE VR application
DPRSLPVR (pin28)=0 => 1 phase CCM mode
DPRSLPVR (pin28)=1 => 1 phase DE mode

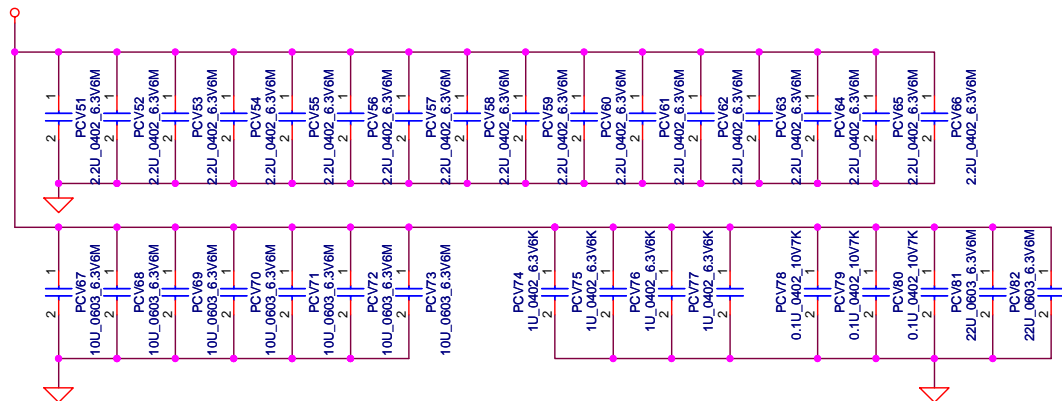


Module model information:
ISL62881C_V1A for IC
ISL62881C_V1B for SW

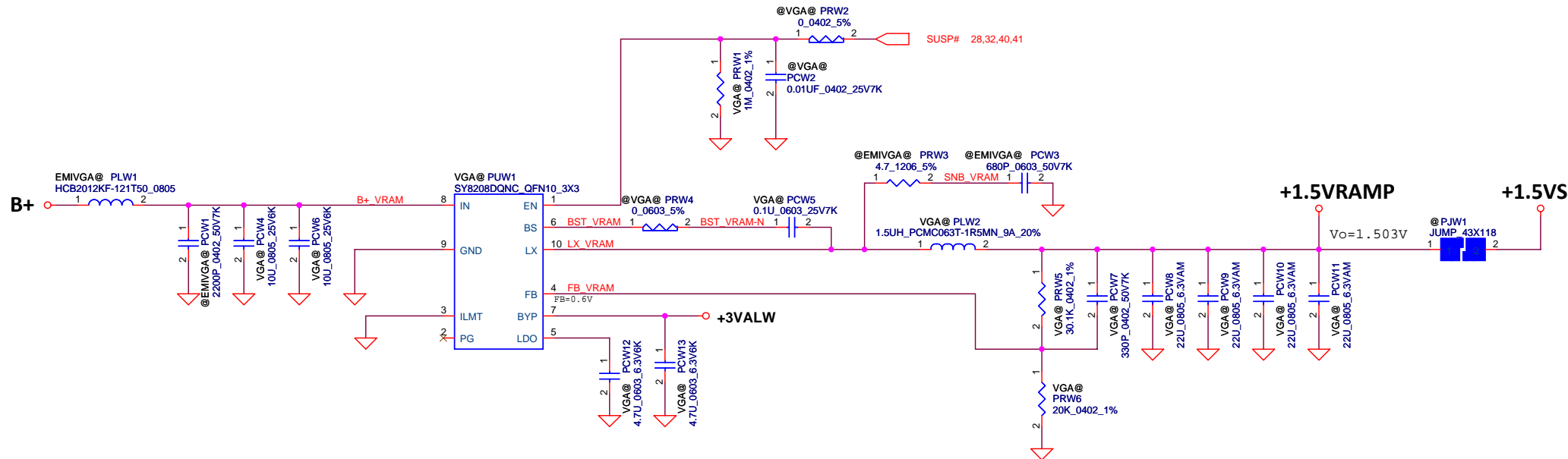
TDC 21A
Peak Current = 31.5A
OCP Current = 37.8A
Load line disable

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+VGA_CORE



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